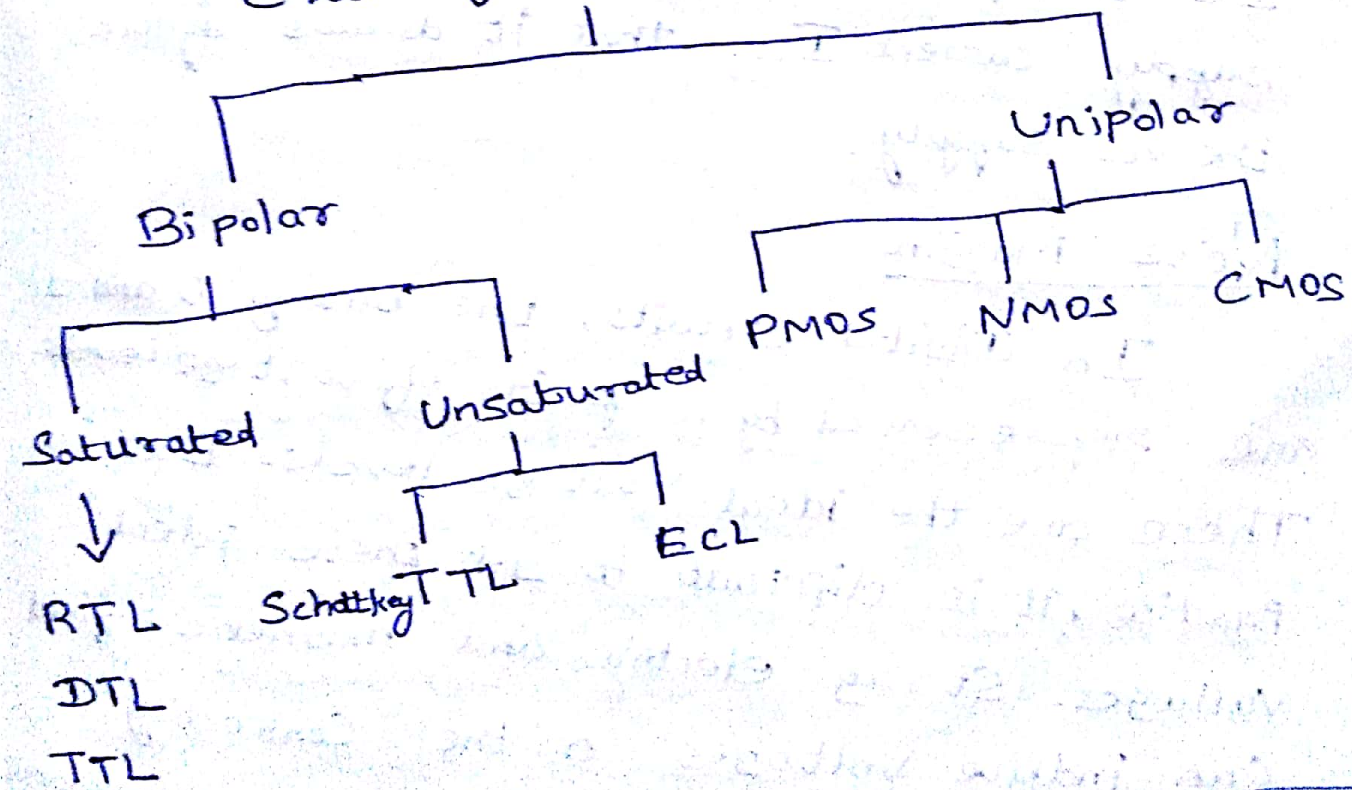
CE 8351 DIGITAL LOGIC CIRCUITS

UNIT-I NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES

Review of number systems - binary codes, error detection and correction codes (Parity and Hamming code). - Digital logic families - Comparison of RTL, DTL, TTL, ECL and MOS families - operation characteristics of digital logic family.

Digital Logic families

Classification of logic families.



Characteristics of Digital Logic families

Propagation Delay:

It is the time interval between the application of an input pulse and the occurrence of the resulting output pulse.

t_{PLH}: It is the delay time measured when output is changing from logic 0 to logic 1.

t_{PHL}: It is the delay time measured when output is changing from logic 1 to logic 0.

Power Dissipation

The amount of power that an IC dissipates is determined by the average supply current I_{cc} that it draws from the V_{cc} supply.

Noise Margin

In Digital circuits, the binary 0 and 1 are represented by a pair of voltage levels. These are the ideal voltage levels. But in practice, it is difficult to get these ideal voltages. Stray electric and magnetic field can induce voltages on the connecting wires between logic circuits. These unwanted signals are called noise and sometimes cause the voltage at the input to

a logic circuit to drop below $V_{IH(min)}$ or rise above $V_{IL(max)}$ which could produce unpredictable operation.

To avoid this problem due to noise, voltage level $V_{IH(min)}$ is kept at a few fraction of volts below $V_{OH(min)}$ and voltage level $V_{IL(max)}$ is kept above $V_{OL(max)}$ at the design time

$$V_{NH} = V_{OH(min)} - V_{IH(min)}$$

$$V_{NL} = V_{IL(max)} - V_{OL(max)}$$

Fan-in and Fan-out

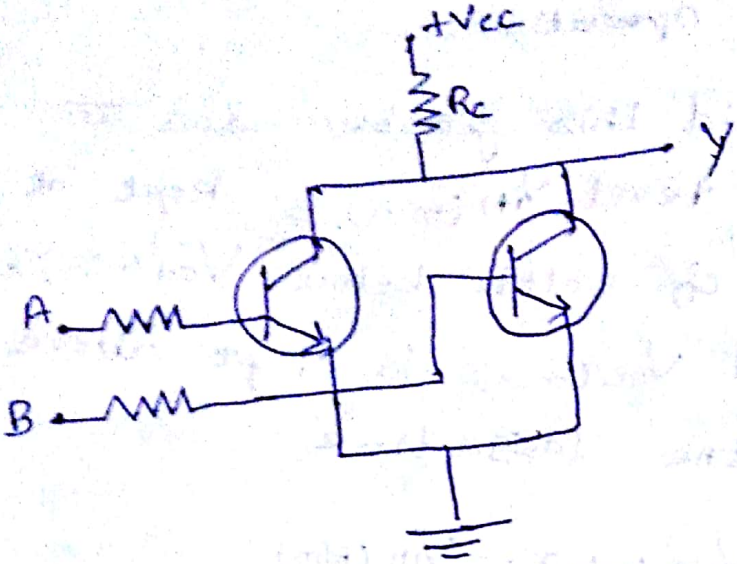
Fan out is defined as the maximum number of inputs of the same IC family that the gate can drive maintaining its output levels within the specified limits.

The fan-in of a digital logic gate refers to the number of inputs.

Speed power product (Figure of Merit)

Measuring and Comparing the overall performance of an IC family is speed power product.

Resistor - Transistor Logic (RTL)



Circuit operation.

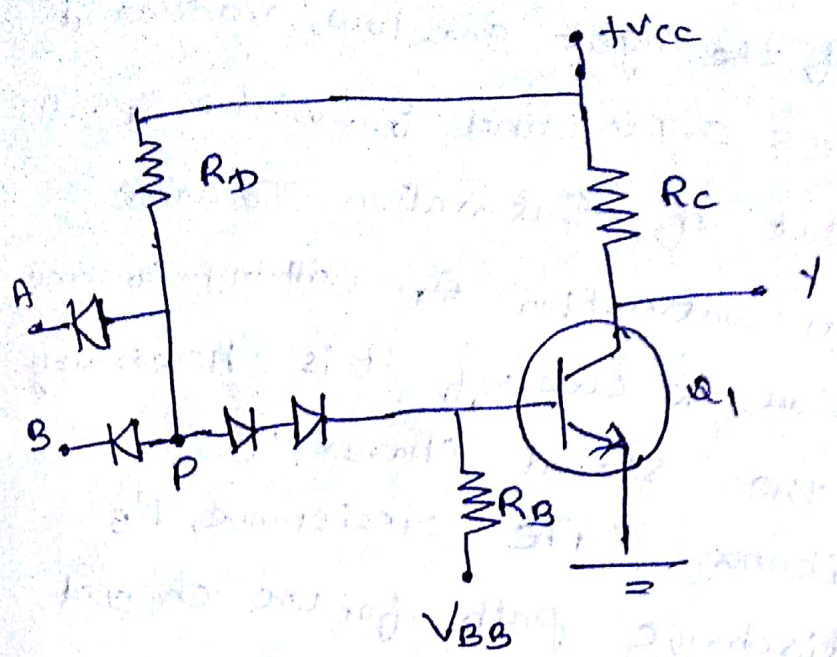
When both the inputs are low, transistors Q_1 and Q_2 are, Cut off and the output is HIGH. A HIGH level on any input drives the corresponding transistor to saturation causing the output to go LOW. It shows the truth table for 2-input NOR Gate.

The Saturation Voltage $V_{CE(sat)}$ for transistor, is 0.2 V. For RTL gates the LOW level output Voltage is 0.2V. In RTL a HIGH level Output Voltage depends on the number of gates connected to the Output. As number of gates Connected to the Output increases, then Output Voltage decreases.

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

NOR Gate.

Diode Transistor Logic (DTL)



A B	Y
0 0	1
0 1	1
1 0	1
1 1	0

Circuit Operation

When both inputs are Low, diode D_A and D_B Conduct resulting 0.7 V at Point P. This 0.7 V is not sufficient to drive transistor Q_1. Therefore Q_1 is cutoff giving output Voltage $V_o = V_{cc}$ (i.e) logic 1. A Low level on any input Cause corresponding diode to conduct resulting Voltage at point P = 0.7V

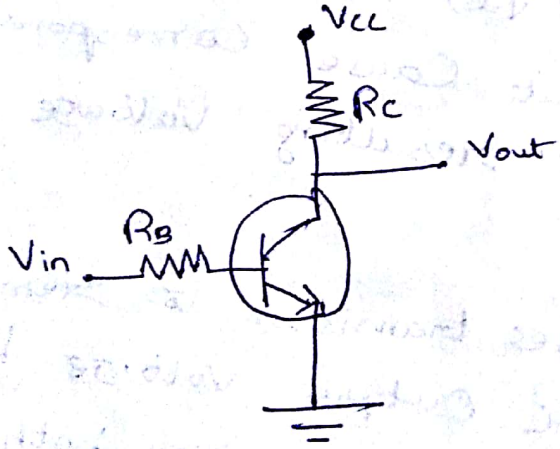
This causes transistor to remain in cutoff and the Output voltage is equal to V_{cc}, logic 1. When both inputs are HIGH, diodes D_A and D_B are reversed biased. This drives Q_1 in saturation giving output voltage $V_{CE(sat)} = 0.2V \approx$ logic 0.

When A & B inputs are HIGH,

transistor Q_1 is driven in Saturation and its base to emitter Junction Capacitance is charged. Now if any of the input goes low, Voltage at point P becomes 0.7 V and transistor Q_1 will try to come out of Saturation. To drive ~~transistor from saturation Or will try to come out of saturation~~. to cut off it is necessary to discharge the stored charge on the internal capacitance. The resistance, R_B provides a discharge path for the charged stored in the transistor.

Transistor Transistor Logic (TTL)

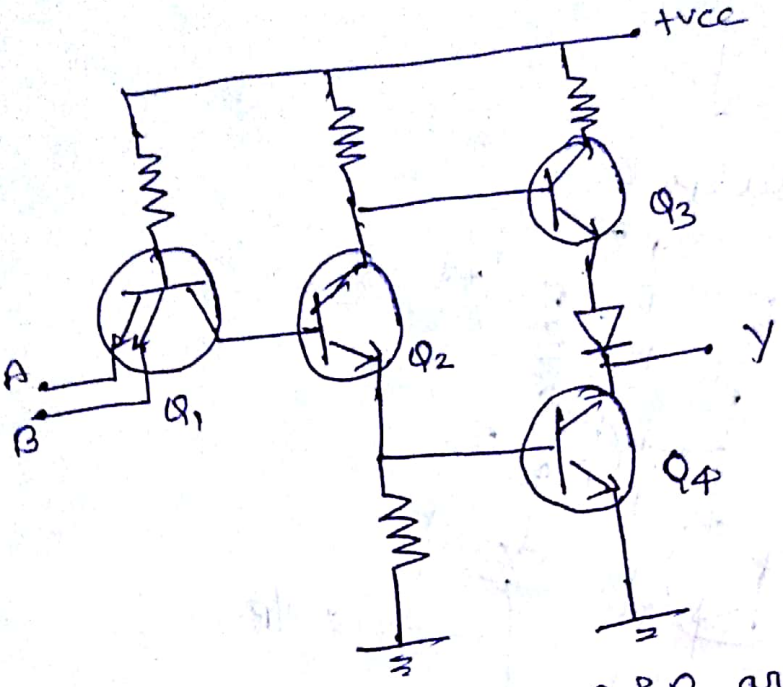
TTL inverter



When the input voltage is low, the output Voltage is HIGH and vice versa.

Vin	Vout
0	1
1	0

2 Input TTL NAND Gates.

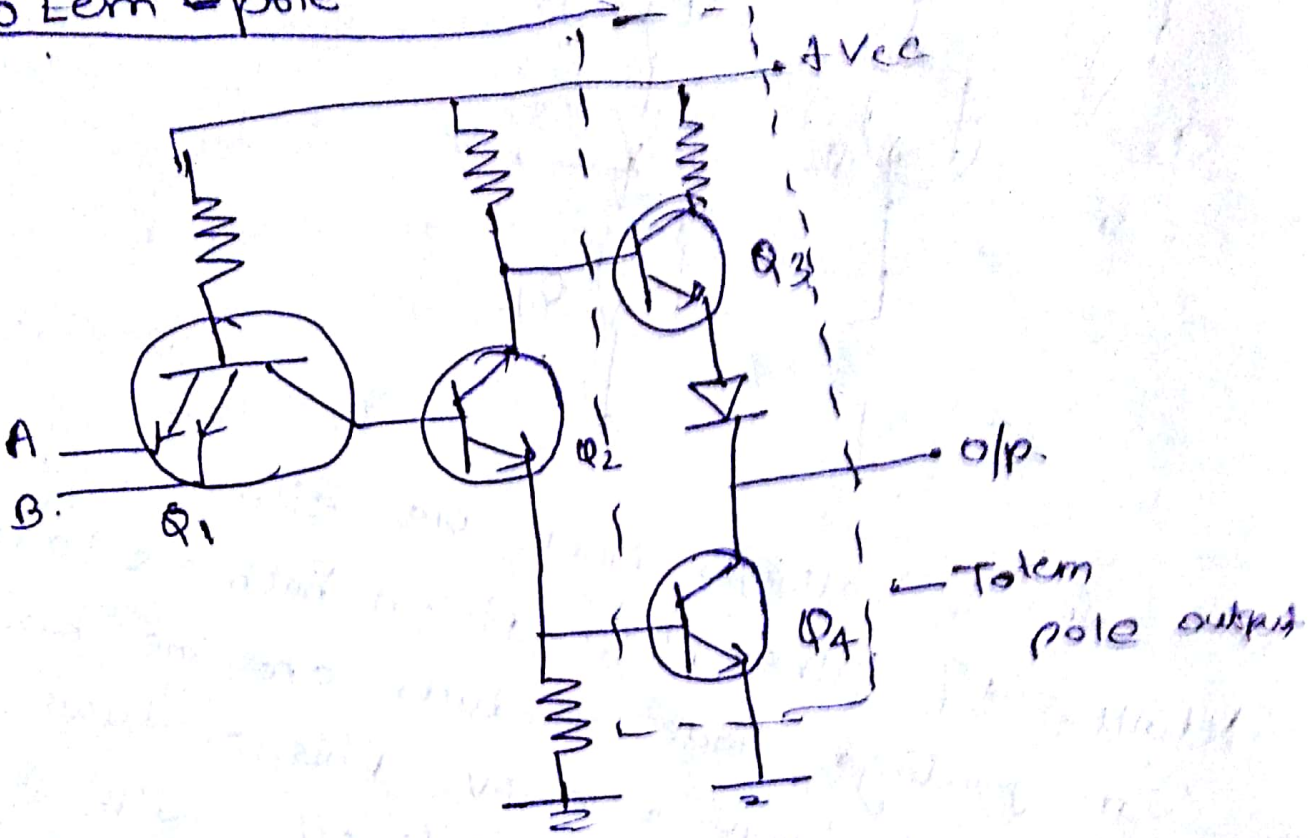


The input Voltages A & B are either low (or) HIGH. If either A (or) B (or) both are low, the corresponding diode conducts and the base of Q_1 is pulled down to 0.7V. This reduces the base of Q_2 to zero. Q_2 cut off. with Q_2 open, Q_4 goes into cutoff and Q_3 base is High. y output is pulled up to HIGH Voltage.

When A & B both are HIGH, emitter diode of Q_1 reverse biased making them off. This causes the Collector diode D_4 to go into forward condition. This forces Q_2 base to go HIGH. In turn Q_4 goes into saturation, producing low output.

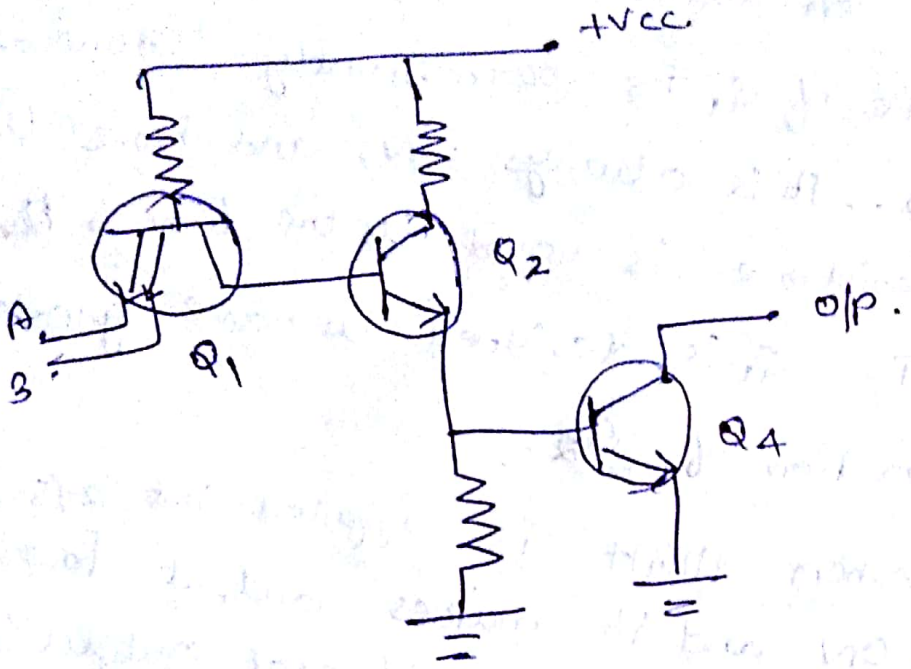
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Totem-pole output



Transistor Q_3 & Q_4 form a Totem pole. Totem pole transistors are used because they produce a LOW output impedance. Either Q_3 acts as an emitter follower. (or) Q_4 is saturated (LOW output). Propagation delay is low in totem-pole TTL logic

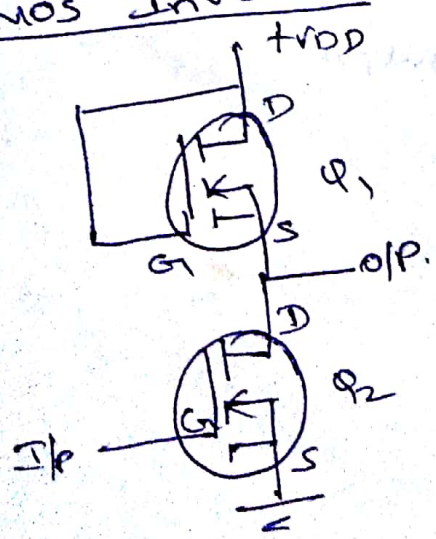
Open Collector output



The output is taken from the open Collector terminal of transistor Q_4. Because the collector of Q_4 is open, a gate like this will not work properly until you connect an external pull-up resistor.

When Q_4 is OFF output is tied to Vcc through an external pull up transistor.

NMOS Inverter

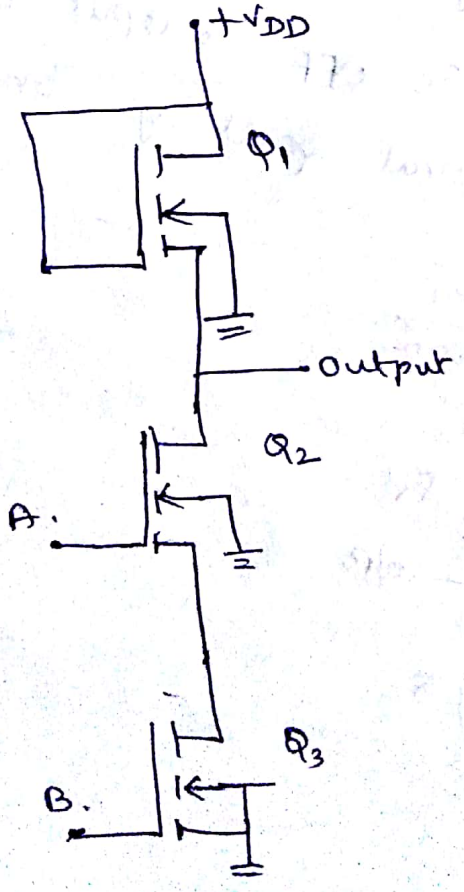


Q_2 is switching MOSFET and Q_1 is load MOSFET. Q_1 acts as load resistance for Q_2. As gate of Q_1 is permanently connected to the V_{DD}., It is always ON, and hence the load resistance is equal to the R_{ON} of Q_2. MOSFET. Q_1 is designed to have greater R_{ON} than R_{ON} of Q_2.

When HIGH is applied ~~at~~ Q_2 is switched ON and it makes output low. when input is low, Q_2 off and Output is high

V_{in}	V_o
0	1
1	0

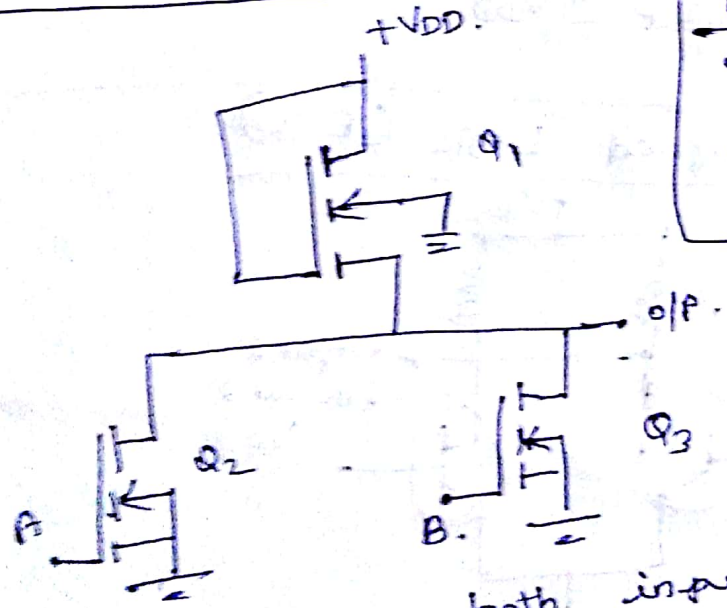
NMOS NAND Gate



If either A or B or both inputs are low, the corresponding MOSFETs are OFF (i.e) the corresponding switches are open and the output is high. If A and B both inputs are high, the corresponding MOSFETs are ON. (i.e) The corresponding switches are closed and the output is low.

A	B	output.
0	0	1
0	1	1
1	0	1
1	1	0

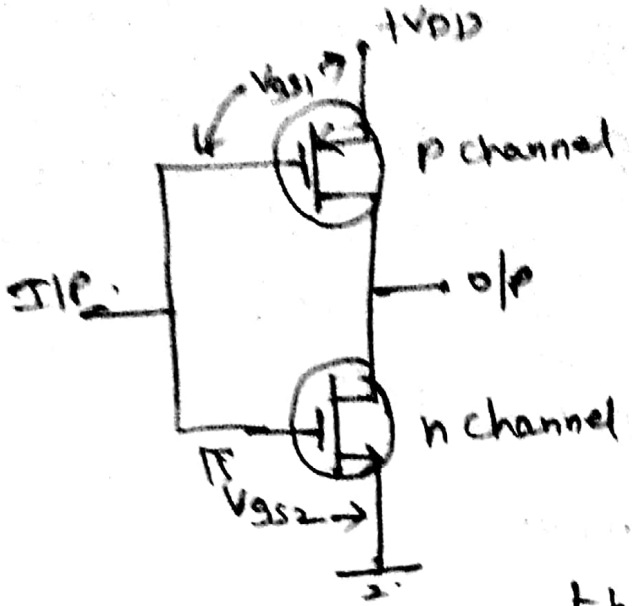
NMOS NOR Gate.



A B	o/p
0 0	1
0 1	0
1 0	0
1 1	0

When either (or) both input are high, the corresponding MOSFETs are ON (i.e) Corresponding switches are closed making the output low. If both inputs are low, both MOSFETs are OFF. (i.e) both switches are open and the Output is high.

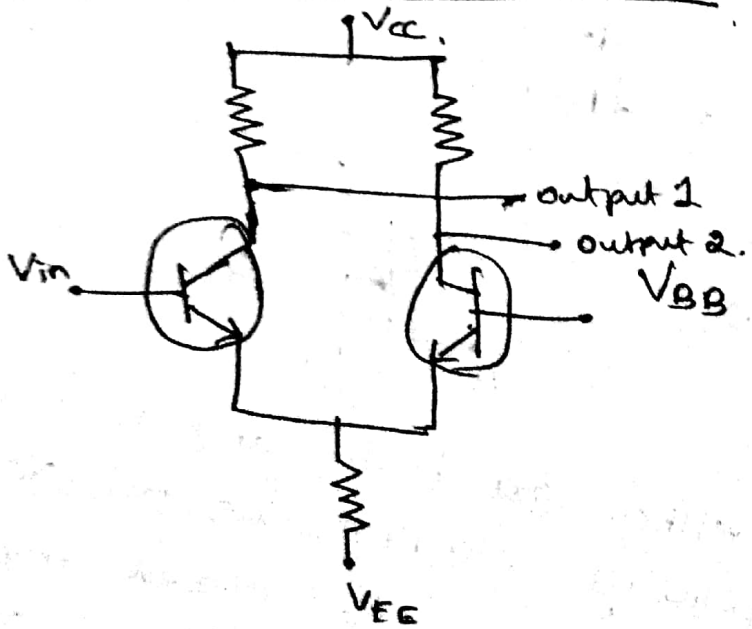
CMOS Inverter



1. When input is HIGH, the gate of Q_1 is at 0V, $V_{gs1} = 0V$. $\therefore Q_1$ is OFF.
$V_{gs2} = V_{DD}$. Therefore Q_2 is ON. $\therefore V_{out} = 0V$.

2. When input is low, $V_{gs2} = 0$, $\therefore Q_2$ off
But Q_1 is p channel. Q_1 is ON.
therefore $V_{out} \simeq V_{DD}$.

Emitter Coupled Logic (ECL)



The Circuit has two outputs: inverting output and non-inverting output

When Vin is high Q_1 is ON, but not Saturated and Q_2 is off. ∴ Vout2 is high. and Vout1 is low.

When Vin is low, Q_2 is ON, but not Saturated and transistor Q_1 is off. Vout1 is high and Vout2 is low

Comparison between Various Digital logic families

Parameter	RTL	DTL	TTL	ECL	MOS
Components used	Resistor & Transistor	Resistor, diode & Transistor	Resistor, diode & Transistor	Resistor and Transistor	MOSFET
Circuit	Simple	Moderate	Complex	Complex	Moderate
Noise Margin	Nominal	Good	Very good	Good	Very Good
Fan-out	Low	Medium	More	High	50.
Power dissipation	12	8-12	10	40-55	0.1
Basic gate	NOR	NAND	NAND	OR-NOR	NAND/NOR
Propagation delay.	12	30	10	2	70.
Applications	Absolute	Absolute	Laboratory instruments	used in high speed switching applications	Used in portable instrument where battery supply is used.
Clock rate	8	12-30	15-60	60-400	5.
Number of functions	High	High	Very High	High	Low.