# EC6202 - Electronic Devices and Circuits

→ Unit I deals with the structure, operation, characteristics of PN junction diode, LED, Laser diodes, Zener diodes and about half and full wave rectifiers

→ Unit - II deals with the structure, operation and characteristics of various transistors like BJT, JFET, MOSFET and Thyristors and IGBT

→ Unit - III deals with the small signal model and analysis of CE, CB, CC amplifiers and gain and frequency response of BJT and MOSFET.

→ Unit IV includes the operation, Gain and frequency response of multistage amplifier and differential amplifier

→ Unit - V deals with the information about Shunt feedback, negative feedback, positive feedback and various types of Oscillators like Wien bridge, Hartley, Colpitts and Crystal Oscillators.

→ Initially diode has been invented which has a characteristics of uncontrolled turn on and turn-off. Their on and off states are controlled by power supply

→ The first introduced power electronic device is the Silicon Controlled rectifier

→ Then different types of thyristor device have been established

→ The thyristor has the characteristics of controlled

turn on and they remain in on-state due to regen action. But they can be turned off by a power circuit

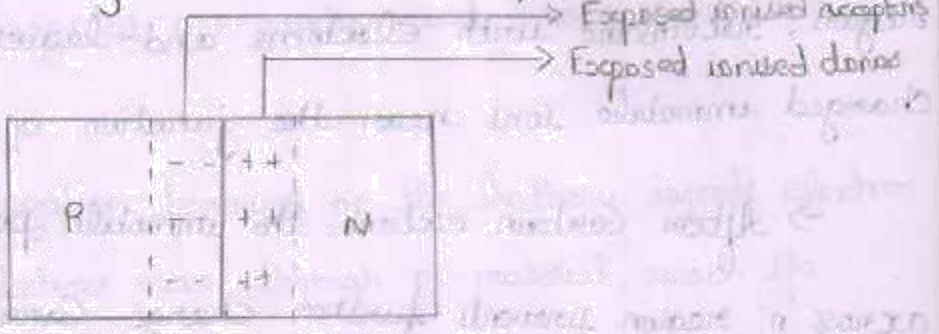
→ Then the controllable switches have been used has the characteristics of controlled turned on and turn off properties which includes various transistors like BJT MOSFET, GTO, IGBT.

→ The power semiconductor devices are used in power electronic circuits, used as freewheeling diode ac to dc conversion, for recovery of trapped energy also as switches in dc choppers and inverters.

JUNCTION DIODE

→ In a piece of Semiconductor material if one half is doped with P-type impurity and the other half is doped by N-type impurity, a P-N Junction is formed

→ The plane dividing the two halves (or) planes are called junction




→ A small amount of pentavalent impurities such as arsenic, antimony (or) phosphorous are added to the semiconductor to get N-type semiconductor

→ The addition of pentavalent impurity increases the number of electrons in the Conduction band.

→ As a result, the number of electrons far exceeds the number of holes, therefore, electrons are the majority carriers and holes are the minority carriers in N-type semiconductor.

→ A small amount of trivalent impurity such as aluminium, boron are added to pure semiconductor to get the P-type semiconductor.

→ This impurity increases the number of holes in the valence band. Therefore holes are the majority carriers and

→ At the junction there is a tendency for the free electrons to diffuse over to P-side and holes to N-side. This process is called diffusion.

→ When the free electrons diffused from 'n' side into 'P' side, it recombine with the holes and leaves a negatively charged immobile ions near the junction of 'P'.

→ Similarly, the holes diffusing from 'p' region into 'n' region, recombine with electrons and leaves the positively charged immobile ions near the junction of 'p' 'n'.

→ After certain extent, the immobile positive ions deposited across 'n' region prevents further charge carriers diffusion from 'P' region into 'n' regions. Similarly, the immobile negative ions deposited across 'P' region prevents further charge carriers diffusion from 'n' region into 'P' region. This immobile ions forms a region called depletion region.

→ The existence of these immobile ions develops the potential difference across the junction, this potential acts as a barrier for further conduction between the junction. This potential is called barrier potential (or) cut in Voltage.

→ The cut in Voltage for Germanium is 0.3 V and 0.7 V for Silicon diodes.

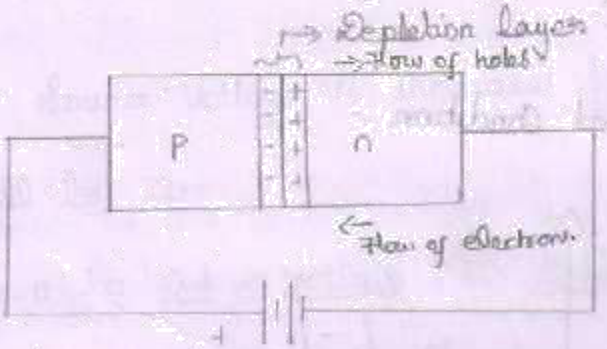
OPERATION :

i) Under forward bias Condition :

→ When positive terminal of the battery is connected to P-type and negative terminal of the battery to the N-type, the P-N junction is forward biased.

→ Positive terminal of the battery sucks electrons from P material leaving holes there. These holes travel through P material towards the negative charge at p-n junction and partly neutralised the negative charge.

→ Similarly, negative terminal of the battery injects electron into n layers. These electrons move through n-material, reach the p-n junction thereby partly neutralising the positive charge which results in reduction of depletion region.




ii) Under Reverse bias Condition

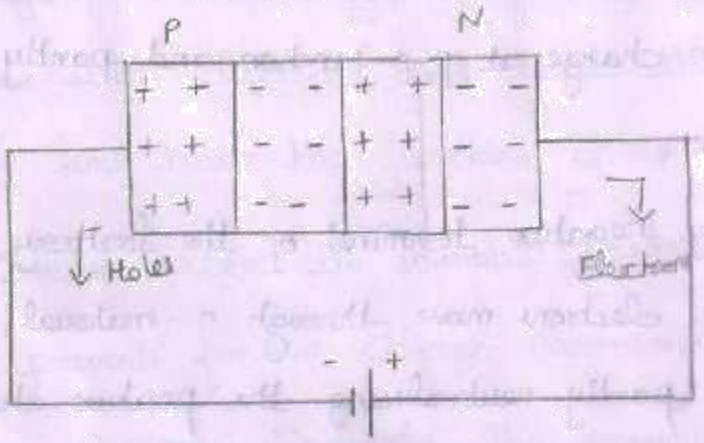
→ When the negative terminal of the battery is connected to P-type and positive terminal of the battery is connected to N type, the bias applied is known as reverse bias.

→ During reverse biased Condition, the holes in the P-side are attracted towards negative terminal of the battery and the electrons in the N-side are attracted towards positive terminal of the battery.

→ As a result, the width of the depletion region increases. Therefore the electric field produced is in the same direction similar to the electric field of the potential barrier.

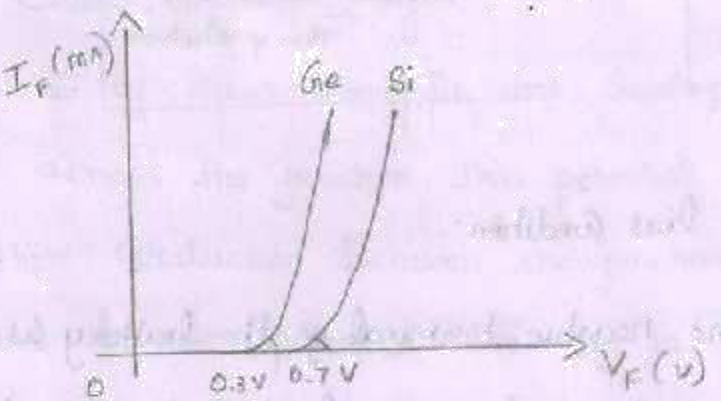
→ Due to this effect the width of the potential barrier will increase which prevents the flow of majority carriers.

→ This is the operation performed by a PN junction diode during reverse bias condition.




V-I characteristics :

i) Under forward biased condition :




→ A plot between voltage and current gives the V-I characteristics of PN junction diode.

→ $V_0$ → barrier potential

$V_F$ → forward voltage

i) $V_F < V_0$

→ When forward Voltage ($V_F$) increases, the forward Current ($I_F$) is almost Zero

→ This is because, the potential barrier prevents holes from P region and electrons from N region to flow across depletion region in the opposite direction.

ii) $V_F > V_0$

→ During this Condition, the potential barrier at the junction disappears completely and as a result the holes Cross the junction from P type to N type and the electrons Cross the junction from N type to P type and hence a large amount of Current will flow in the external Circuit

Operation:

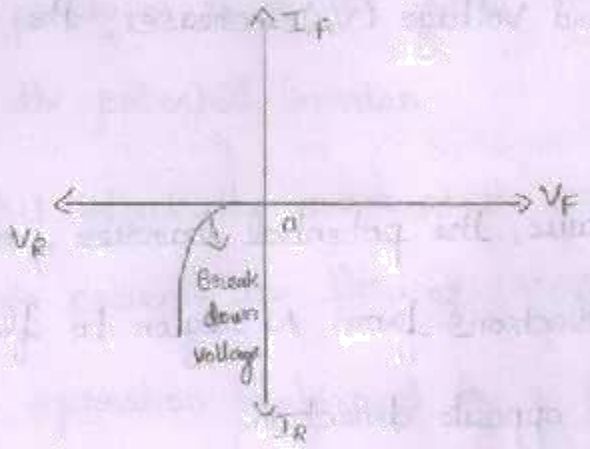
→ When the Source Voltage Vs, increases from Zero Value. the diode Current will be Zero

→ From $V_S = 0$ to cut in Voltage (or) threshold Voltage, the forward diode Current is very Small

→ Beyond the Cut in Voltage, the diode Current rises rapidly and the diode will start to Conduct

→ the Cut in Voltage for Silicon is 0.7 V and for Germanium it is 0.3 V

ii) Under reverse biased Condition:




→ Under reverse biased condition, no current should flow in the external circuit. But practically, a very small amount of current will flow.

→ This is because that during the reverse biased condition, the thermally generated holes in the P-region are attracted towards the negative terminal of the battery and the electrons in the N-region are attracted towards the positive terminal of the battery. At the same time, the electrons in the P region and holes in the N region move towards the junction and will flow towards their majority carrier side which results in a small reverse current. This current is known as reverse saturation current.

→ The magnitude of the reverse saturation current will depend on the junction temperature.

→ For large applied reverse bias, the electrons from N type towards positive terminal of the battery will acquire energy to gain velocity in order to dislodge the valence electrons

$$C_T = \left| \frac{dQ}{dV} \right|$$

$dQ \Rightarrow$ increase in charge caused by change in voltage $dV$

where $C_T$ is called transition (or) space charge (or) barrier (or) depletion region capacitance

DIFFUSION CAPACITANCE:

→ Diffusion capacitance is defined as the rate of change of change of injected charge with applied voltage

$$C_D = \frac{dQ}{dV}$$

→ $dQ \Rightarrow$ change in number of minority carriers stored outside the depletion region

$dV \Rightarrow$ change in voltage across diode

$C_D \Rightarrow$ Diffusion capacitance

→ Diffusion capacitance will exists during forward biased condition.

→ The value of diffusion capacitance is larger than the transition capacitance

→ The value of $C_D$ increases exponentially with diode forward current

→ The value of $C_D$ is directly proportional to diode forward current and inversely proportional to frequency.

→ The value of $C_D$ ranges from 10 to 1000 pF

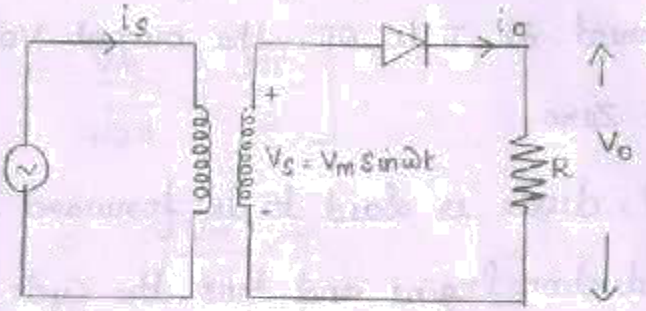
RECTIFIERS:

→ Rectification is the process of conversion of alternating input voltage to direct output voltage

⇒ Rectifier will convert ac power to dc power.

⇒ It may be of half wave rectifier and full wave rectifier

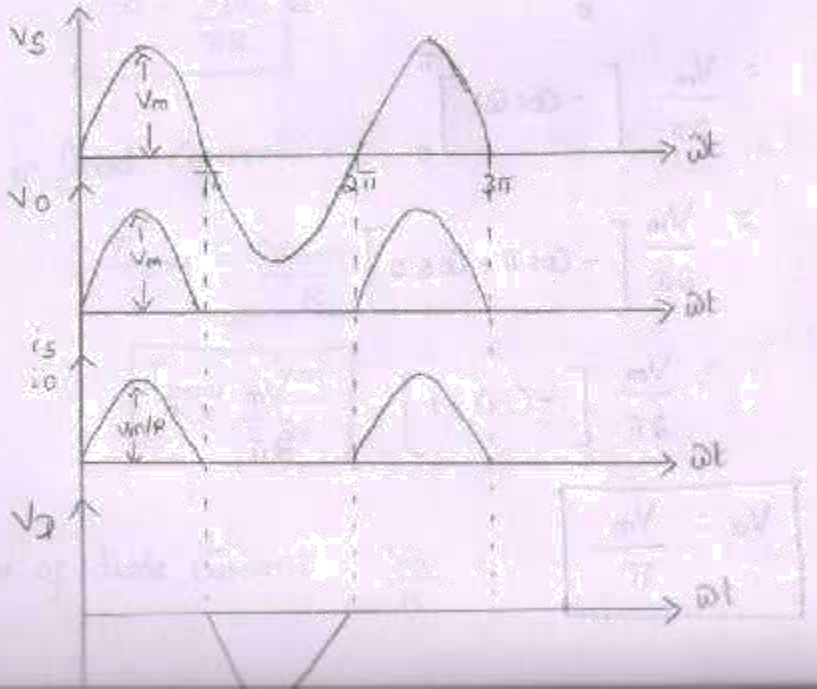
Half wave rectifier:




→ In the half wave rectifier circuit, for one cycle of supply voltage, there is one half cycle of output

→ The circuit consist of a transformer, a diode and the load. The load may be R, $R_L$ (or) $R_L$ with flywheel diode

Operation:-



→ During positive half cycle, diode is forward biased, and it is said to be Conducting from $\omega t = 0^\circ$ to $\omega t = \pi$.

→ During this process, the output voltage, $V_o = V_s$ (source Voltage) and the load Current will be $i_o = V_o / R$.

→ At $\omega t = \pi$, the output Voltage will be zero and for resistive load, the load current will also be zero.

→ After $\omega t = \pi$, the source Voltage will become negative and the diode D is said to be reverse biased and therefore it will get turn off and will go into blocking state

→ During the period $\omega t = \pi$ to $2\pi$, the output Voltage and output Current will be Zero

→ After $\omega t = 2\pi$, diode is said to be forward biased and therefore the Conduction begins and thus the cycle repeats.

→ During the Conduction of diode, the diode Voltage will be Zero

Average Value of output Voltage

$$V_o = \frac{1}{2\pi}\left[\int_0^{\pi} V_m \sin\omega t \, d\omega t\right]$$

$$= \frac{V_m}{2\pi}\left[-\cos\omega t\right]_0^{\pi}$$

$$= \frac{V_m}{2\pi}\left[-\cos\pi + \cos 0\right]$$

$$= \frac{V_m}{2\pi}\left[-(-1)+1\right] = \frac{V_m}{2\pi} \times 2$$

$$\boxed{V_o = \frac{V_m}{\pi}}$$

Rms Value of output Voltage

$$V_{orms} = \left[ \frac{1}{2\pi} \int_0^{\pi} V_m^2 \sin^2 \omega t \, d\omega t \right]^{1/2}$$

$$= \frac{V_m}{\sqrt{2\pi}} \left[ \int_0^{\pi} \frac{1 - \cos 2\omega t}{2} \, d\omega t \right]^{1/2}$$

$$= \frac{V_m}{\sqrt{4\pi}} \left\{ \left[ \frac{\omega t - \sin 2\omega t}{2} \right]_0^{\pi} \right\}^{1/2}$$

$$= \frac{V_m}{\sqrt{2\pi}} \left\{ \frac{\pi - \sin 2\pi}{2} - \frac{0 \sin 0}{4} \right\}^{1/2}$$

$$= \frac{V_m}{\sqrt{2\pi}} \left[ \frac{\sqrt{\pi}}{2} \right]$$

$$= \sqrt{\frac{V_m^2}{4\pi} \times \pi}$$

$$\boxed{V_{orms} = \frac{V_m}{2}}$$

Average Value of load Current,

$$I_o = \frac{V_o}{R}$$

$$\boxed{I_o = \frac{V_m}{\pi R}}$$

Rms Value of load Current

$$I_{orms} = \frac{V_{orms}}{R}$$

$$\boxed{I_{orms} = \frac{V_m}{2R}}$$

Peak Value of diode Current $= \frac{V_m}{R}$

Peak Inverse Voltage:

⇒ It is defined as the maximum voltage that appears across the diode during its blocking state.

$$\boxed{PIV = V_m = \sqrt{2} \times V_s}$$

Input power factor:

$$I.P.F = \frac{\text{Power delivered to load}}{\text{Input VA}}$$

$$= \frac{V_{0rms} \times I_{0rms}}{V_s \times I_{0rms}}$$

$$= \frac{V_{0rms}}{V_s} = \frac{\sqrt{2}V_s}{2V_s}$$

$$\boxed{I.P.F = 0.707 \text{ lag}}$$

Full Wave Rectifier Output dc power:-

$$P_{dc} = V_0 I_0 = \frac{V_m \cdot I_m}{\pi^2}$$

Output ac power:

$$P_{ac} = V_{0rms} \cdot I_{0rms} = \frac{V_m I_m}{4}$$

Rectifier efficiency:

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{V_m I_m}{\pi^2} \times \frac{4}{V_m I_m}$$

$$= \frac{4}{\pi^2}$$

$$\eta = 40.53\ \%$$

Ripple factor:

⇒ It is defined as the ratio of rms value of ac voltage (or) current to the average value of ac voltage (or) current

$$RF = \frac{\sqrt{V_{rms}^2 - V_o^2}}{V_o} = \frac{V_r}{V_o}$$

$$= \frac{\sqrt{\left(\frac{V_m}{2}\right)^2 - \left(\frac{V_m}{\pi}\right)^2}}{V_o} = \frac{0.3856 \times V_m}{\frac{V_m}{\pi}}$$

$$= 0.3856 \times \pi$$

**R.F. = 1.211**

Transformer Utilisation Factor:

→ It is defined as the ratio of dc power delivered to the load to the VA rating of the transformer

$$TUF = \frac{P_{dc}}{V_s I_s} = \frac{V_m I_m}{\pi^2} \times \frac{2\sqrt{2}}{V_m I_m}$$

**TUF = 0.2865**

Advantage:

→ It is a simple and low cost circuit

Disadvantages:

→ Has low rectification efficiency
→ High ripple factor
→ Transformer is not fully utilised
→ Regulation is poor

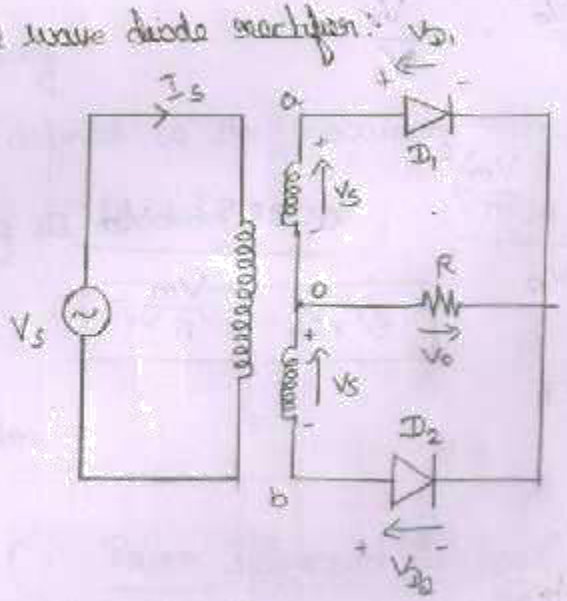
Full Wave rectifier:

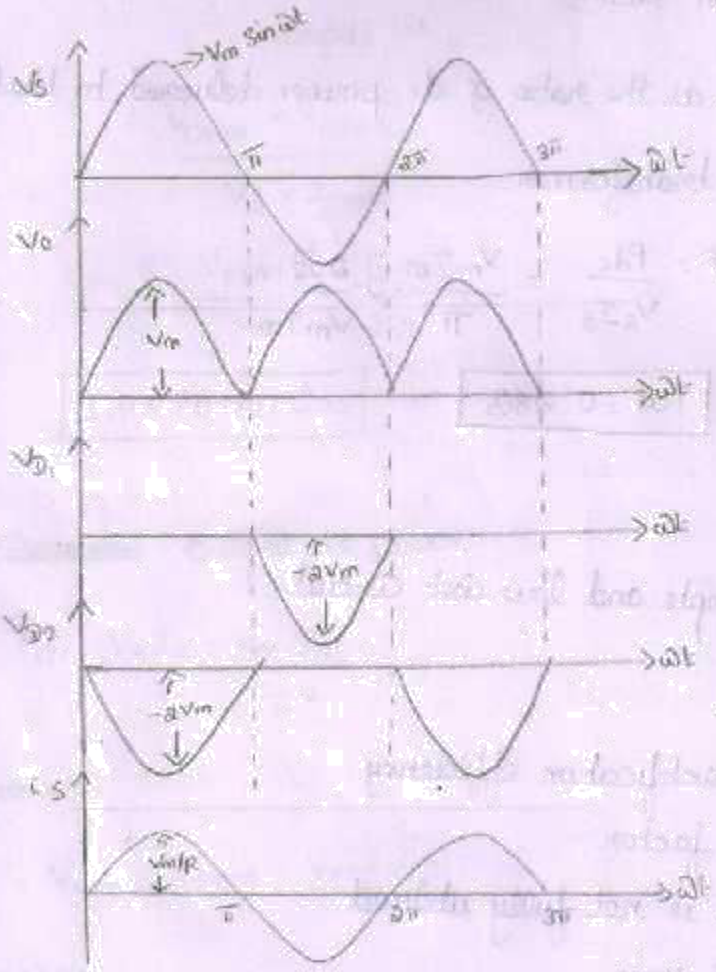
→ It is of two types

i) Centre tapped full wave diode rectifier
ii) Full wave diode bridge rectifier

→ In the full wave rectifier, for one cycle of source voltage, there are two pulses of output voltage

Centre tapped full wave diode rectifier:




Operation:

-> When 'a' is positive with respect to 'B', the diode $D_1$ Conducts for $\pi$ radians

-> In the next half cycle, 'b' is positive with respect to 'a', therefore the diode $D_2$ Conducts up from $\pi$ to $2\pi$ radians

-> Simultaneously when 'a' is positive with respect to 'b', $D_2$ is subjected to reverse voltage of $2V_s$. In the next half cycle,

diode D, experiences a reverse voltage of $2V_s$

Average output voltage. $V_o = \frac{1}{\pi}\int_0^{\pi} V_m \sin \omega t \, d\omega t$

$$= \frac{V_m}{\pi}\left[-\cos\omega t\right]_0^{\pi} = \frac{V_m}{\pi}\left[-\cos\pi + \cos 0\right]$$

$$= \frac{V_m}{\pi}\left[-(-1)+1\right]$$

$$V_o = \frac{2V_m}{\pi}$$

Average output current. $I_o = \frac{V_o}{R}$

Rms value of output voltage. $V_{orms} = \left[\frac{1}{\pi}\int_0^{\pi} V_m^2 \sin^2 \omega t \, d\omega t\right]^{1/2}$

$$\boxed{V_{orms} = \frac{V_m}{\sqrt{2}}}$$

Rms value of load current. $I_{orms} = \frac{V_{orms}}{R}$

Output dc power. $P_{dc} = V_o I_o = \frac{2V_m}{\pi} \times \frac{2}{\pi} I_m$

$$P_{dc} = \frac{4}{\pi^2} V_m I_m$$

output ac power. $P_{ac} = V_{orms} I_{orms} = \frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}} = \frac{V_m I_m}{2}$

$$P_{ac} = \frac{V_m I_m}{2}$$

Rectifier efficiency. $\eta = \frac{P_{dc}}{P_{ac}} = \frac{4}{\pi^2} \times V_m I_m \times \frac{2}{V_m I_m} = \frac{8}{\pi^2}$

$$\eta = 0.8106$$

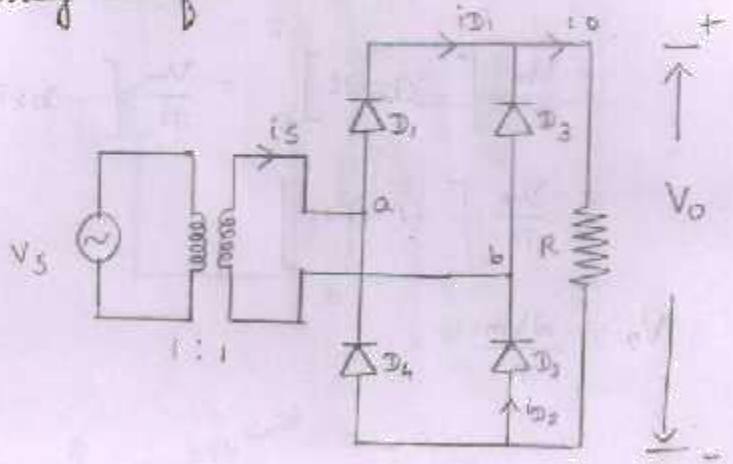
Ripple factor. $RF = \frac{V_r}{V_o} = \frac{\sqrt{V_{orms}^2 - V_o^2}}{V_o} = \sqrt{\left(\frac{V_m}{\sqrt{2}}\right)^2 - \left(\frac{2V_m}{\pi}\right)^2} = \frac{0.3077 V_m \times \pi}{2V_m}$

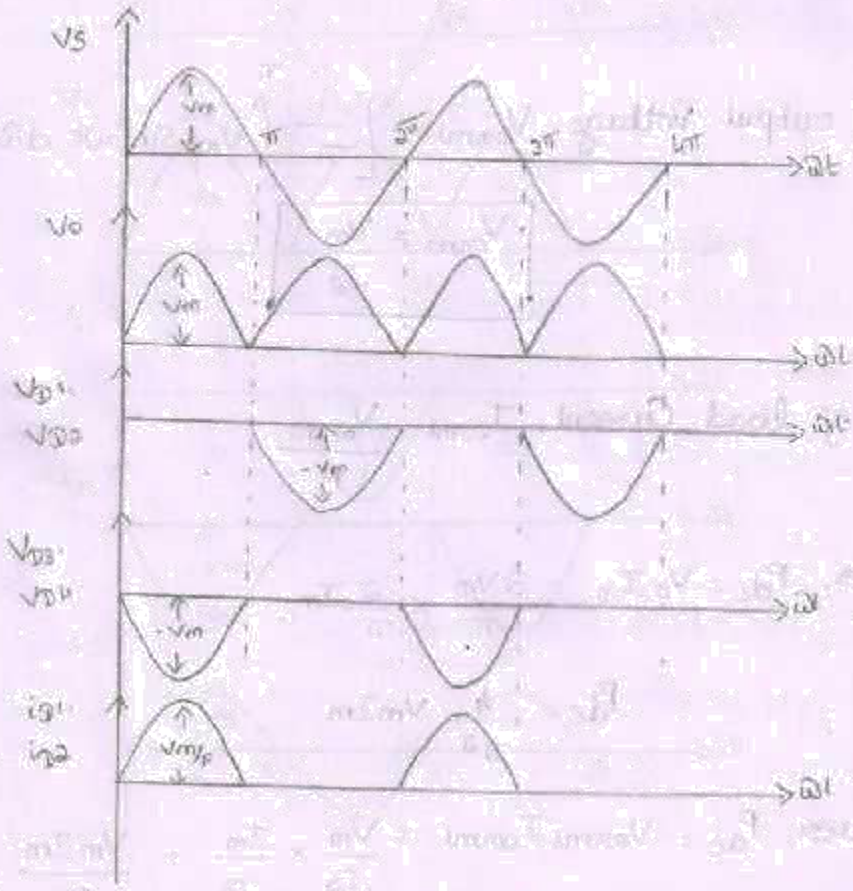
$V_o$

RF = 0.483.

TUF = 0.672.

Full Wave Bridge Rectifier :-



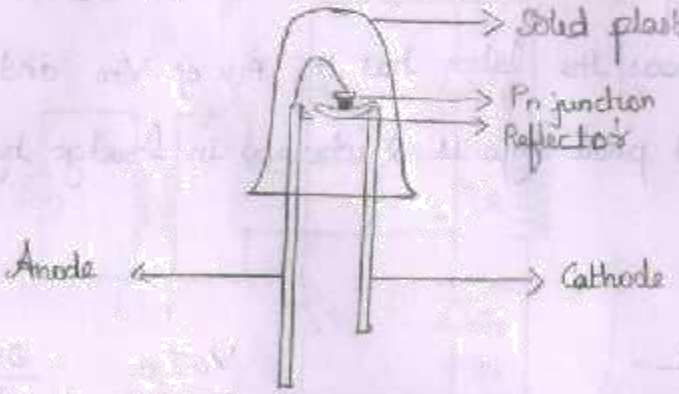

⇒ When 'a' is positive with respect to 'b', the diodes $D_1$ and $D_3$ will Conduct with a voltage of $V_{ab}$

⇒ During this operation, the diodes $D_2$ and $D_4$ is subjected to reverse voltage of the value $V_S$

⇒ When 'b' is positive with respect to 'a', the diodes $D_2$ and $D_4$ will Conduct with a voltage of $V_{ba}$ and the diodes $D_1$ and $D_3$

Symbol:

Construction:




→ The pn junction diode is mounted on a cup shaped reflector.

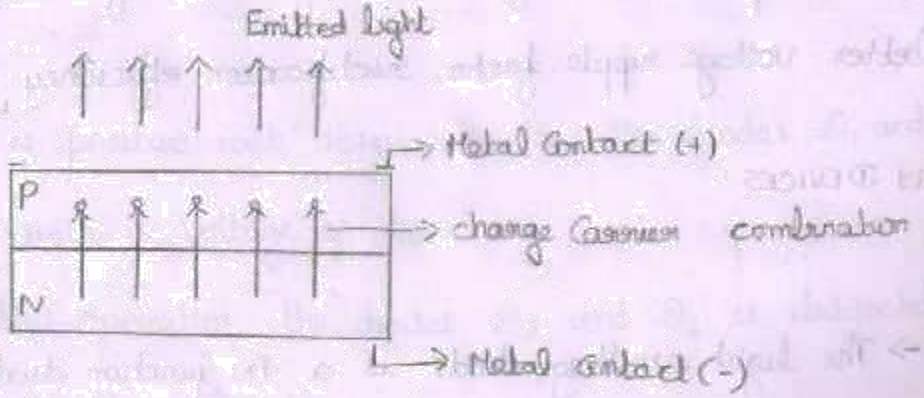
→ Wire connection will be provided for anode and cathode connection.

→ The whole device is encapsulated in an epoxy lens. The lens can be either coloured (or) colorless.

→ The type of the pn junction material will determine the color of the light emitted from the energised LED.

→ Some of the LED's have glass particles embedded in the epoxy lens to diffuse the emitted light and thereby increasing the viewing angle of the device.

Structure:




→ An N-type layer is grown on a substrate and a P-type layer is deposited on it by diffusion. The process of Carrier recombination will take place in the P layer.

is subjected to a reverse voltage of $V_s$

→ The major difference between the mid point full wave rectifier and full wave bridge rectifier is that the former has the peak inverse voltage of $2V_m$ whereas the later has the PIV of $V_m$. and the number of diodes used in mid point type is 2 whereas in bridge type is 4.

TUF:

$$TUF = \frac{P_{dc}}{VA \text{ rating of transformer}} = \frac{V_o I_o}{V_s I_s} = \frac{\frac{2V_m}{\pi} \times \frac{2I_m}{\pi}}{\frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}}$$

$$= \frac{4V_m I_m}{\pi^2} \times \frac{2}{V_m I_m} = \frac{8}{\pi^2}$$

$$\boxed{TUF = 0.8106}$$

→ From the above equation, it is clear that the transformer is utilised efficiently in bridge rectifier than the mid point type

→ The bridge rectifier type is economical.

→ PIV is defined as the maximum voltage that a diode can withstand under reverse biased condition

→ Compared to half wave rectifier, the full wave rectifier has better voltage ripple factor, rectification efficiency and TUF.

DISPLAY DEVICES:

LED:

→ The light emitting diode is a PN junction diode. It works based on the principle of electroluminescence which emit light when the PN junction diode is forward biased

→ In order to allow more emitted surface area for the light to escape, the metal anode connections are made at the outer edges of P layer.

→ To reduce the reabsorption problem, domed lenses are used

Operation:

→ When the LED is forward biased, the electrons and holes move towards the junction and the recombination will take place.

→ As a result of the recombination process, the electrons lying in the conduction bands of N region will fall into the holes lying in the valence band of P region.

→ The difference in the energy level between the conduction band and valence band is radiated in the form of light energy.

→ Thus the recombination of electrons and holes will generate the light and their excess energy is transferred to an emitted photon.

→ The brightness of the light is directly proportional to the forward bias current.

→ The wavelength of the emitted light depends on the energy gap of the material

→ The efficiency of generation of light increases with increase in the injected current and with a decrease in temperature.

→ As the colour of the emitted light depends on type of material, if Gallium arsenide is used, there will be infrared radiation. If Gallium phosphide is used, the emitted light will be in red (or) green colour. The emitted light will be red (or) yellow in colour if Gallium arsenide phosphide is used.

→ For the protection purpose of LED, resistance of 1 kΩ (or) 1.5 kΩ must be connected in series with the LED.

Characteristics:

→ The operating voltage level of LED is from 1.5 V to 3.3 V.

→ The operating current is in the range of some tens of milliamperes.

→ The switching speed is 1 ns

→ The power requirement ranges from 10 to 150 mW with a lifetime of 1,00,000+ hours.

Applications:

→ Calculators.

→ Digital meters

→ Intercoms

→ Burglar alarm systems

→ digital watches.

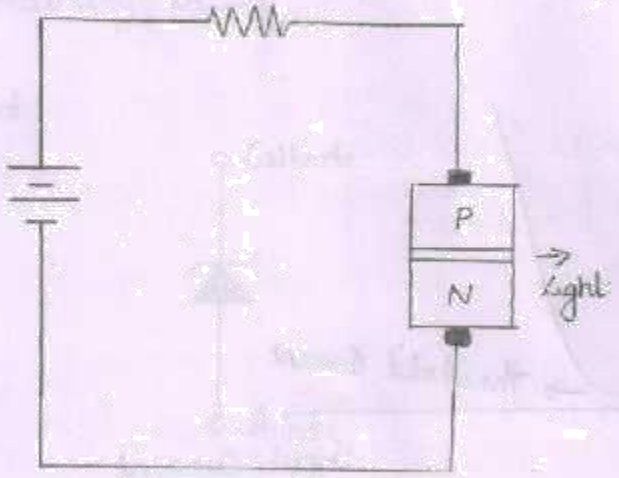
LASER DIODES

→ LASER stands for light amplification by stimulated emission of radiation.

→ The laser emits radiation with a single wavelength (or) a very narrow band of wavelengths which is in the range of 1 μm to 100 μm in width.

→ The emitted laser light has a single colour i.e., it is monochromatic and it is also a coherent type of light.

Structure




→ A pn junction of gallium arsenide or Combination of gallium arsenide Combined with other materials is manufactured with a precisely defined length related to the wavelength of the light to be emitted.

→ The ends of the junction are each polished to a mirror surface and usually have an additional reflective coating.

→ One end is partially reflective so that light can pass through when lasing occurs.

Operation :

→ When free electrons recombine with holes, the photons which is emitted reflect back and forth between the mirror surfaces.

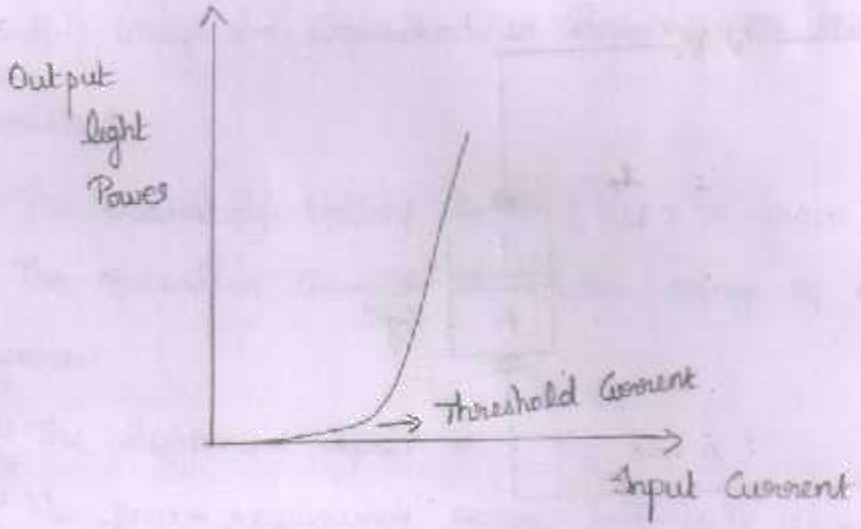
→ Since the photons bounce back and forth, they induce an Avalanche effect.

→ The region between the mirrored ends acts like a cavity that filters the light and purifies it colour.

→ One of the mirror surfaces is semitransparent. From this surface, a fine thread like beam of photons emerge out.

→ All the photons of laser light have same frequency and also they are in phase.

Characteristics:




→ The above characteristics between the Input Current and Output light power shows that this device has a well defined threshold level of forward current at which

→ Below the threshold value, the device exhibits low level of spontaneous emission.

Application:

Bar Codes

Fiber optic Communication

playing music from a Compact disc.

Zener diode

→ In a normal pn junction diode, when the reverse voltage reaches the breakdown voltage value, the current through the junction and the power dissipated at the junction will be high.

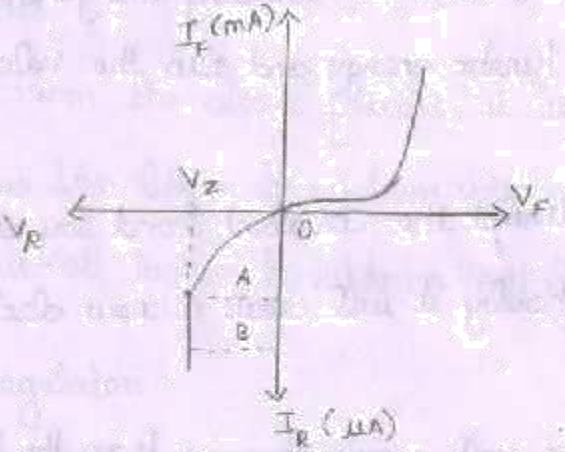
→ This phenomenon is very dangerous and the diode will also be get damaged.

→ In order to overcome this problem, the diodes are constructed with adequate power dissipation capabilities which will allow them to operate even in breakdown region.

→ Zener diode is one of the above type which is heavily doped than the ordinary diode.

Circuit Symbol:


V-I characteristics




→ Under forward biased Condition, the operation of Zener diode is similar to the PN junction diode.

→ Under reverse biased Condition, a small leakage Current will flow. If the reverse voltage across Zener diode is increased, a value of voltage is reached at which reverse breakdown occurs, which is indicated by a sudden increase of Zener Current.

→ The breakdown voltage value depends upon the amount of doping. If the diode is heavily doped, depletion layer will be thin and therefore the breakdown will occur at lower reverse voltage and also the breakdown voltage is sharp.

⇒ The lightly doped diode has a higher breakdown voltage.

⇒ The sharp increasing current under breakdown condition is due to

Avalanche breakdown

Zener breakdown.

Avalanche breakdown :-

⇒ When there is increase in the applied reverse bias, the field across the junction also increases.

⇒ Thermally generated carriers while crossing the junction will acquire more amount of kinetic energy and also the velocity of the carriers also increases.

⇒ The electrons will disrupt the covalent bond by colliding with the immovable ions and thereby it will create a new electron - hole pairs.

⇒ Again the new carriers will acquire energy from the field and they will collide with immovable ions and hence another electron - hole pairs will generate.

⇒ The above process repeats again and results in the generation of more amount of charge carriers within a short time.

⇒ This process of carrier generation is known as **Avalanche multiplication**. It will result in the flow of large amount of current.

Zener breakdown :-

⇒ When the P and N regions are doped heavily, the width of the depletion region will increase when the applied voltage is 6V or below 6V and also the field across the depletion region will increase which will make the condition suitable for zener breakdown.

→ Because of strong electric fields, rupture of Covalent bonds will take place at the junction of PN junction diode when P and N regions are heavily doped

→ The newly created electron hole pairs will increase the reverse current in reverse biased PN junction diode

→ The increase in the current will take place during reverse bias below 6V for heavily doped diodes

→ The Zener breakdown voltage will be high for lightly doped diodes.

→ From the above process, it is clear that Zener breakdown will occur for Zener breakdown voltage and Avalanche breakdown will occur at higher breakdown voltage.

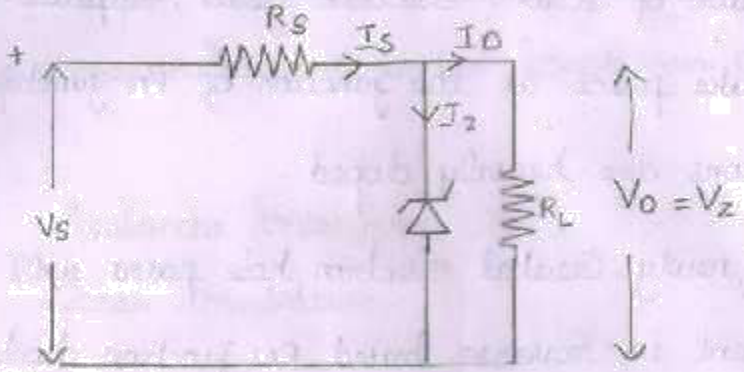
Zener as regulator :-

→ From the characteristics of Zener diode, it is clear that eventhough the current through the diode increases, the voltage across the diode remains almost constant.

→ Due to the above characteristics, the voltage across the diode can be used as a reference voltage and hence this diode can be used a voltage regulator.

→ Voltage regulator is nothing but a electrical or electronic device which maintains the voltage of a power source within acceptable limits.

→ The voltage regulator is needed to keep the voltages within the range that can be tolerated by the equipment. & automatically maintains a constant voltage level.




→ For operating Zener diode as a voltage regulator, it must satisfy two requirements

i) it should be reverse biased with a voltage greater than the breakdown voltage (or) Zener voltage

ii) a series resistor $R_S$ must be connected in series in order to limit the reverse current through the diode below its rated value.

→ For operating Zener diode as a voltage regulator, it must be reverse biased as long as the input voltage does not fall below Zener breakdown voltage, the voltage across the diode will be constant and therefore the load voltage will also be constant

→ If $V_Z$ is the voltage across Zener diode, then the source current will be

$$I_S = \frac{V_S - V_Z}{R_S}$$

→ Output current,

$$I_O = \frac{V_Z}{R}$$

→ Current through Zener diode, $I_Z = I_S - I_O$

Unit-1 Completed 20/8/20

turn on and they remain in on-state due to regen action. But they can be turned off by a power circuit

→ Then the controllable switches have been used has the characteristics of controlled turned on and turn off properties which includes various transistors like BJT MOSFET, GTO, IGBT.

→ The power semiconductor devices are used in power electronic circuits, used as freewheeling diode ac to dc conversion, for recovery of trapped energy also as switches in dc choppers and inverters.

UNIT-II

# TRANSISTORS

→ Transistors are the devices which can be turned on and turned off by the application of control signals. i.e, they can be used as a controllable switches.

## BJT :-

→ BJT is a three terminal semiconductor device whose operation depends upon the interaction of both majority and minority carriers and hence its name is Bipolar.

→ It is a Current Controlled device

## Construction :-

→ The BJT is a three layer two junction semiconductor device

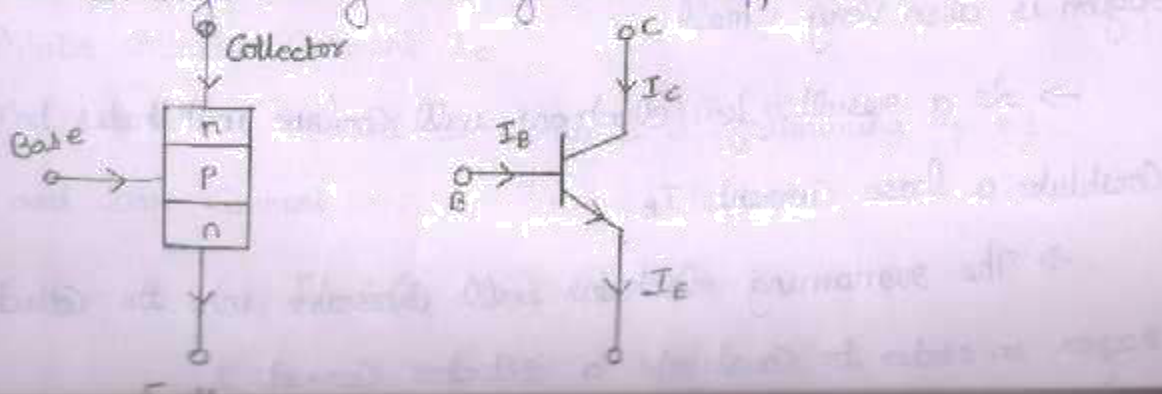
→ The BJT has three terminals namely Collector, Emitter and base

→ The BJT has two Configuration namely

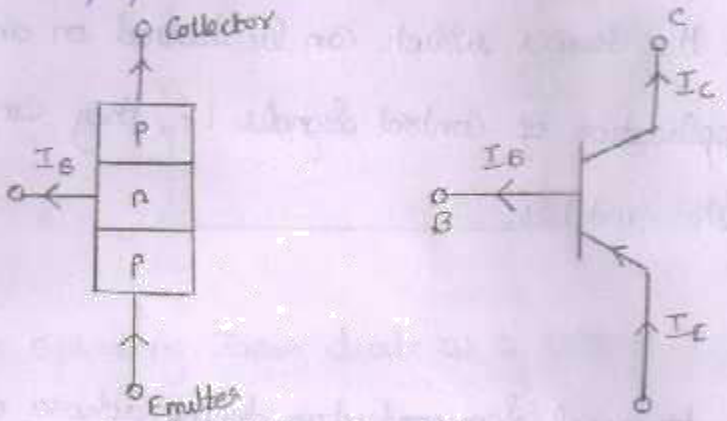
npn transistor

pnp transistor

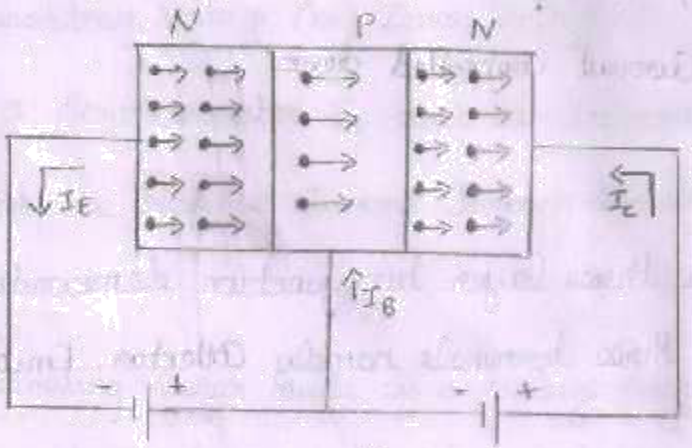
→ When one p-region is sandwiched between two n region, npn transistor Configuration is obtained. This type of Configuration is easy to manufacture and it is cheaper also and hence this type is used in high voltage and high current application.



→ When one of the n region is sandwiched between two P regions, a pnp transistor is obtained.




Operation of NPN transistor:




→ When forward bias is applied to the emitter base junction of a NPN transistor, a lot of electrons will crossover from the emitter region to the base region.

→ Since the base is lightly doped with p-type impurity, the number of holes in the base region is very small and therefore the number of electrons combines with holes in the P type base region is also very small.

→ As a result, few electrons will combine with holes to constitute a base current $I_B$.

→ The remaining electrons will crossover into the collector region in order to constitute a collector current $I_C$.

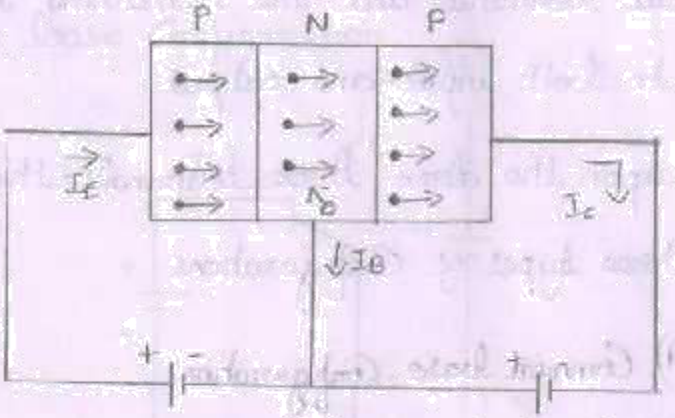
→ The emitter current is obtained by summing up of base and collected current.

$$I_E = -(I_C + I_B)$$

→ In the external circuit of NPN BJT, the emitter current is given by,

$$I_E = I_C + I_B$$

Operation of PNP transistor




→ When forward bias is applied to the emitter base junction of PNP transistor, more number of holes will crossover to the base region from the emitter region since the base is lightly doped with N-types of impurity.

→ Since the number of electrons in the base region is very small, the number of holes combined with electrons in N type base region is also very small and this combination will constitute a base current $I_B$.

→ The remaining holes will crossover into the collector region to constitute collector current $I_C$.

→ The emitter current is obtained by summing up of collector and base current

$$I_E = (I_C + I_B)$$

→ In the external Circuit of PNP BJP, the emitter Current is given by.

$$I_E = I_C + I_B$$

Types of Configuration :-

→ When a transistor is to be Connected to a Circuit, one of the terminal is used as input terminal, other terminal Can be used as output terminal and the remaining third terminal is Common to both input and output.

→ Depending upon the above three terminals the BJT Can be Connected in three types of Configurations.

i) Common base Configuration
ii) Common emitter Configuration
iii) Common Collector Configuration

Common base Configuration :-

→ also called as grounded base Configuration

→ Input terminal → emitter
output terminal → Collector
Common terminal → base

Common Emitter Configuration :-

→ also called as grounded emitter Configuration

Input terminal - base
output terminal → Collector
Common terminal - Emitter

Common Collector Configuration

→ also called as grounded Collector Configuration

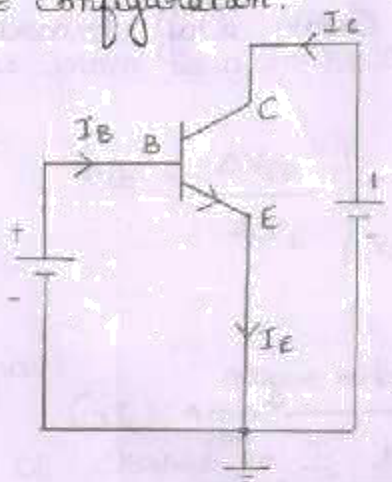
Input terminal - base

output terminal - emitter

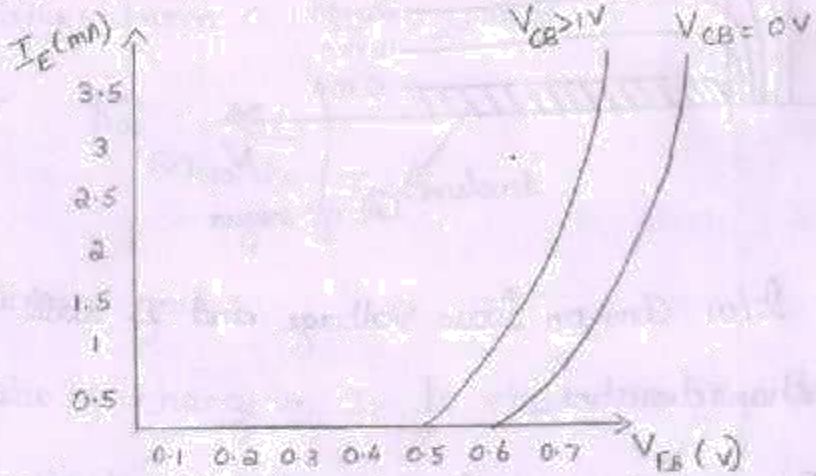
Common terminal - Collector

Characteristics of BJT under different Configuration

1) Common base Configuration:-




Input Characteristics:-




→ A plot between the Emitter base voltage and Emitter current will give the I/p characteristics under CB Configuration

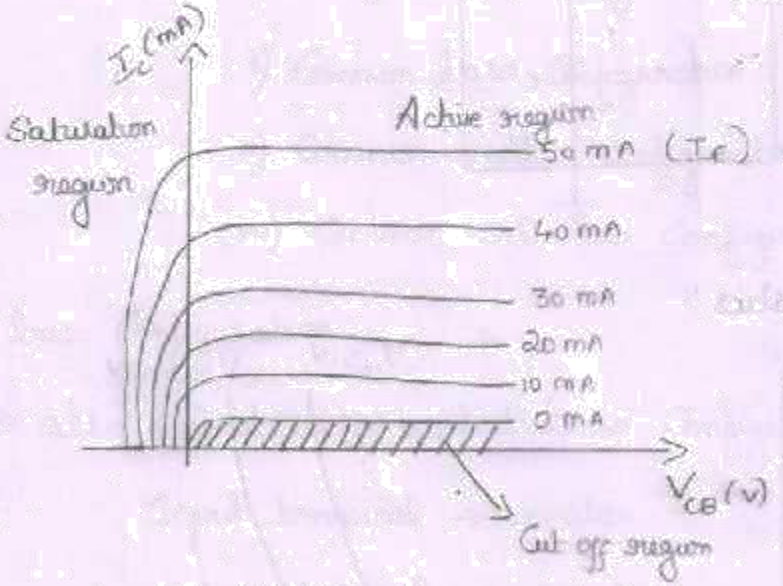
→ The Input characteristics is obtained by the keeping the $V_{CB}$ as Constant at Zero volt and by increasing $I_E$ from zero gradually by increasing $V_{EB}$

→ The junction will behave as a forward biased diode, when $V_{CB}$ is zero and EB junction is forward biased and as a result $I_E$ increases rapidly with small increase in $V_{EB}$.

→ The width of the base region will get decreased when $V_{CB}$ is increased by keeping $V_{EB}$ as constant which result in increase of $I_E$.

→ Because of this, the curve shift towards the left when $V_{CB}$ is increased.

Output characteristics:




→ A plot b/w common base voltage and $I_C$ will give the o/p characteristics

→ Here, By keeping $I_E$ is kept constant by adjusting $V_{EB}$, the $V_{CB}$ is increased and $I_C$ is noted for each $I_E$. and it is repeated for different $I_E$.

→ $I_c$ is independent of $V_{CB}$ and the curves are parallel to the axis of $V_{CB}$ for constant value of $I_E$. and also it is noted that $I_c$ flows when $V_{CB}$ is zero.

Transistor parameters:

a) Input impedance:

→ Ratio of change in emitter voltage to change in emitter current with collector voltage as constant

→ Ranges from 20Ω to 50Ω

$$h_{ib} = \left.\frac{\Delta V_{EB}}{\Delta I_E}\right|_{V_{CB} \text{ constant}}$$

b) Output admittance:

→ Ratio of change in $I_c$ to change in $V_{CB}$ by keeping $I_E$ as constant

→ Ranges from 0.1 to 10 μmhos

$$h_{ob} = \left.\frac{\Delta I_c}{\Delta V_{CB}}\right|_{I_E \text{ constant}}$$

c) Forward current gain:

→ Ratio of change in $I_c$ to change in $I_E$ by keeping $V_{CB}$ as constant

→ Ranges from 0.9 to 1.0

$$h_{fb} = \left.\frac{\Delta I_c}{\Delta I_E}\right|_{V_{CB} \text{ constant}}$$

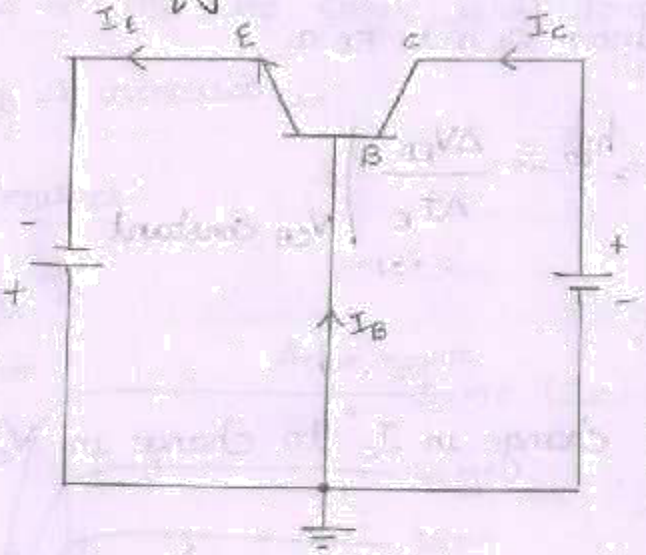
d) Reverse voltage gain:

→ Ratio of change in $V_{EB}$ to change in $V_{CB}$ with Constant $I_E$.

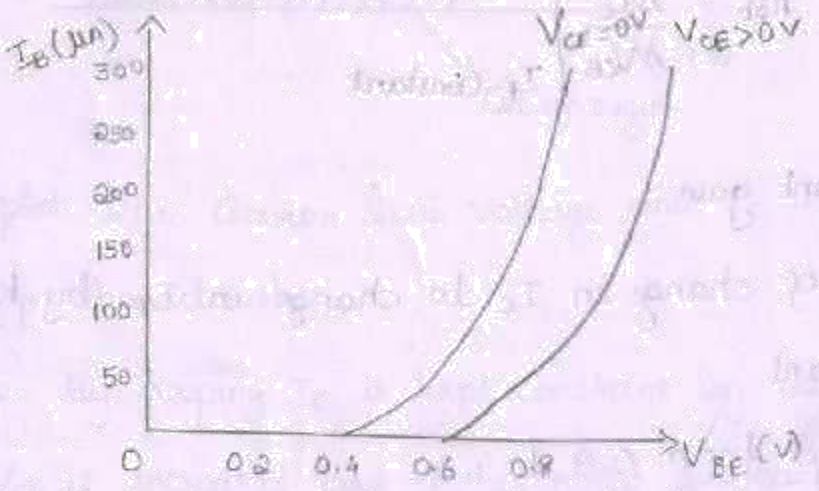
→ It is in the order of $10^{-5}$ to $10^{-4}$

$$h_{rb} = \left.\frac{\Delta V_{EB}}{\Delta V_{CB}}\right|_{I_E \text{ Constant}}$$

ii) Common Emitter Configuration:




Input characteristics:




→ A plot b/w $V_{BE}$ and $I_B$ by keeping $V_{CE}$ as constant will result in Input characteristics.

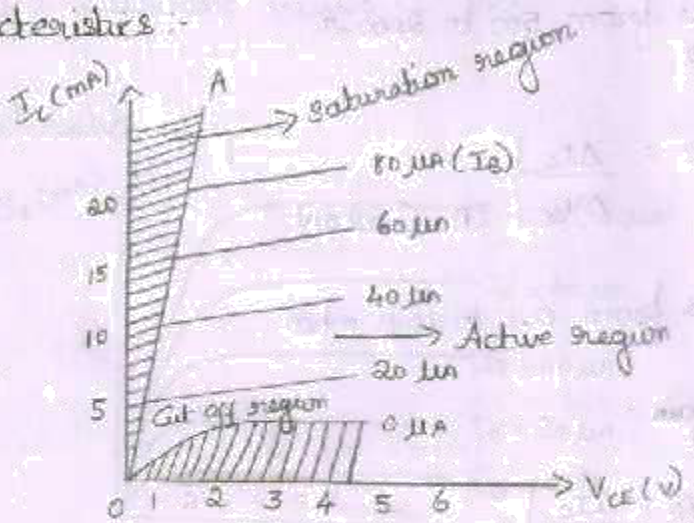
→ By keeping $V_{CE}$ as Constant at Zero volt, $I_B$ is increased from Zero by increasing $V_{BE}$ and the value of $V_{BE}$ is noted

for each value of $I_B$ and the procedure is repeated for large fixed values of $V_{CE}$

→ If $V_{CE} = 0$, the emitter base junction will be forward biased. If $V_{CE}$ is increased the width of the depletion region will increase and therefore the width of the base will decrease which results in decrease in $I_B$

→ When $V_{CE} = 0$, in order to get same $I_b$, $V_{BE}$ should be increased

Output characteristics :-




⇒ A plot b/w $V_{CE}$ and $I_c$ with constant $I_B$ will give the output characteristics

⇒ By keeping $I_B$ as constant by adjusting $V_{BE}$, $V_{CE}$ is increased from zero and $I_c$ is noted for each value of $V_{CE}$.

⇒ It has three regions

Saturation region

Cut off region

active region

→ The part of the curve left of OA is the saturation region and the line OA is the Saturation line. Both junctions are forward biased

→ Region below the curve for $I_B = 0$ is the Cut off region. Both junctions are reverse biased

-> The central region where the curves are uniform in spacing and slope is called active region. In this Emitter base junction is forward biased and Collector base junction is reverse biased

Transistor parameters :-

a) Input Impedance :-

$$h_{ie} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE}\ \text{Constant}}$$

-> ranges from 500 to 2000 $\Omega$

b) output admittance.

$$h_{oe} = \left.\frac{\Delta I_C}{\Delta V_{CE}}\right|_{I_B\ \text{Constant}}$$

-> ranges from 0.1 to 10 $\mu$ mhos

c) forward Current gain :-

$$h_{fe} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\ \text{Constant}}$$

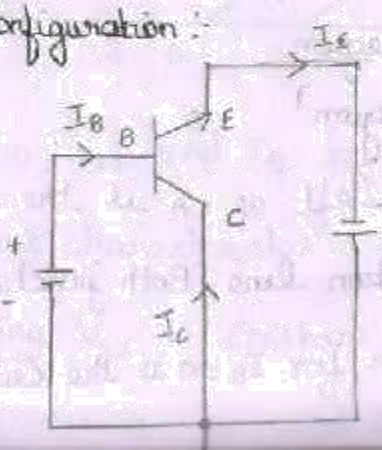
-> ranges from 20 to 200

d) Reverse voltage gain :

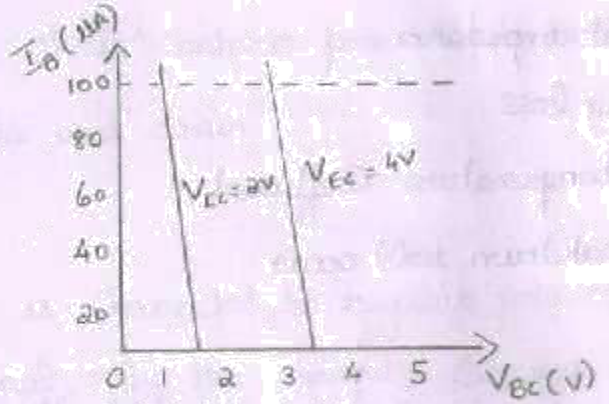
$$h_{re} = \left.\frac{\Delta V_{BE}}{\Delta V_{CE}}\right|_{I_B\ \text{Constant}}$$

-> In the order of $10^{-5}$ to $10^{-4}$

Common Collector Configuration :-

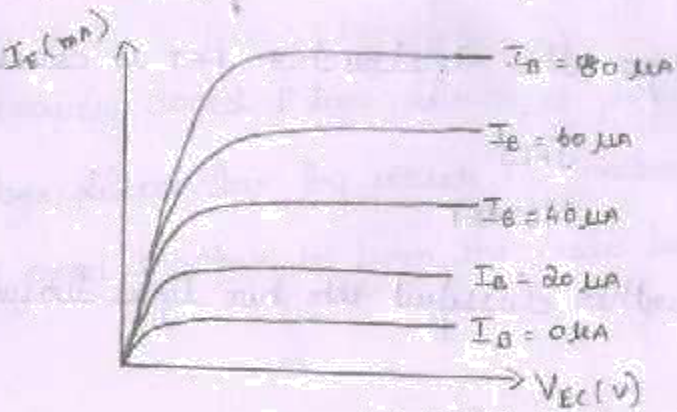


Input characteristics:




→ In this, by keeping $V_{EC}$ as constant, $V_{BC}$ is increased in equal steps and the corresponding increase in $I_B$ is noted which is repeated for different values of $V_{EC}$

Output characteristics:




→ By keeping $I_B$ as constant, $V_{EC}$ is increased in equal steps and the corresponding $I_C$ is noted which gives the output characteristics

Application:

→ Amplifier and Oscillator Circuits
→ Switch in digital Circuits
→ Computers
→ Satellites
→ Communication System

Disadvantage :-

→ has low input impedance
→ High Switching loss
→ has negative temperature Coefficient
→ Secondary breakdown will occur

JFET :

→ Field Effect Transistor is a device in which the flow of the current through the Conducting region is controlled by electric field

→ In this type of device, the Conduction of current is by majority Carriers only, and hence it is a unipolar device

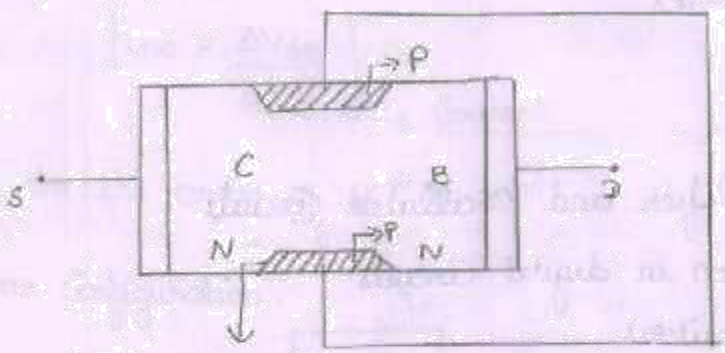
→ Depending upon the Construction, FET is classified into

JFET
MOSFET

→ JFET is further classified into two types based on the majority Carriers

N-channel JFET - Majority Carriers → electrons
P channel JFET - Majority Carriers → holes

Construction :-




→ It Consist of three terminal

Gate
Drain
Source

Disadvantage :-

→ has low input impedance
→ High Switching loss
→ has negative temperature Coefficient
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JFET :

→ Field Effect transistor is a device in which the flow of the current through the conducting region is controlled by electric field.

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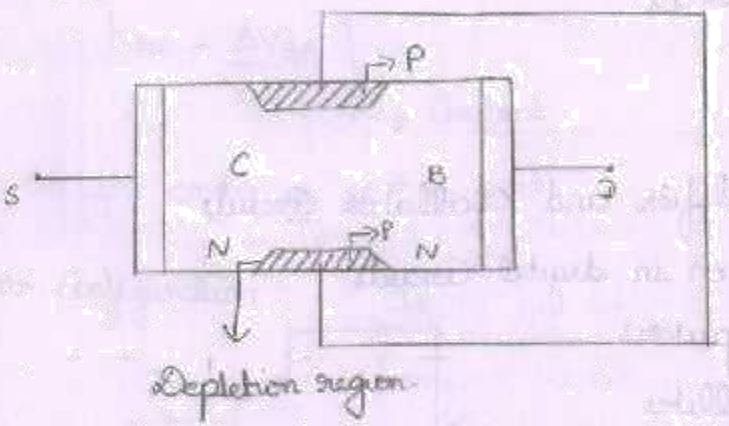
N-channel JFET - Majority Carriers → electrons
P-channel JFET - Majority Carriers → holes

Construction :-




→ It Consist of three terminal

Gate
Drain
Source

→ N-channel JFET has N type bar which is made up of Silicon. The ohmic contacts present at two ends of the bar are called Source and drain.

Source :-

→ It is connected to negative pole of the battery. Through this terminal only the majority carriers (electrons) in the N-type bar enter the bar

Drain :

→ It is connected to positive pole of the battery. The majority carriers will leave the bar through this terminal

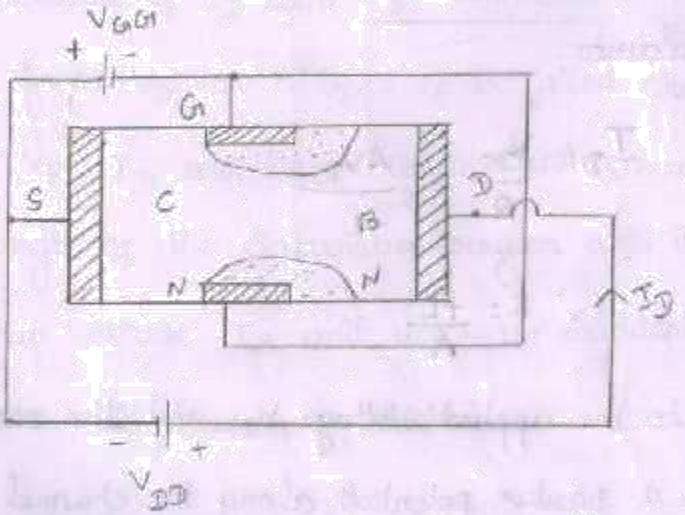
Gate :-

→ A heavily doped P type silicon is diffused on both sides of the N-type silicon bar by which PN junctions are formed. These layers are joined together to form the Gate terminal

Channel :

→ The region BC in the N type bar between the depletion region is called the channel.

Operation :



i) $V_{GS} = 0$ and $V_{DS} = 0$ :-

→ When no voltage is applied between drain and source and gate and source, the thickness of the depletion region around the PN junction will be uniform

ii) $V_{DS} = 0$ and $V_{GS}$ is decreased from zero :-

⇒ In this case, the thickness of the depletion region will be increased since the PN junction is reverse biased

→ This is because, when $V_{GS}$ is decreased from zero, the reverse bias voltage across the PN junction is increased and therefore the thickness of the depletion region in the channel also increases until the two depletion region make contact with each other and the channel in this condition is called cut off and the value of $V_{gs}$ required to cut off the channel is called cut off voltage $V_c$.

iii) $V_{GS} = 0$ and $V_{DS}$ is increased from zero :

⇒ When $V_{GS} = 0$, drain is positive with respect to source. During this condition, electrons (majority carriers) will flow through N-channel from source to drain, and as a result $I_D$ will flow from drain to source.

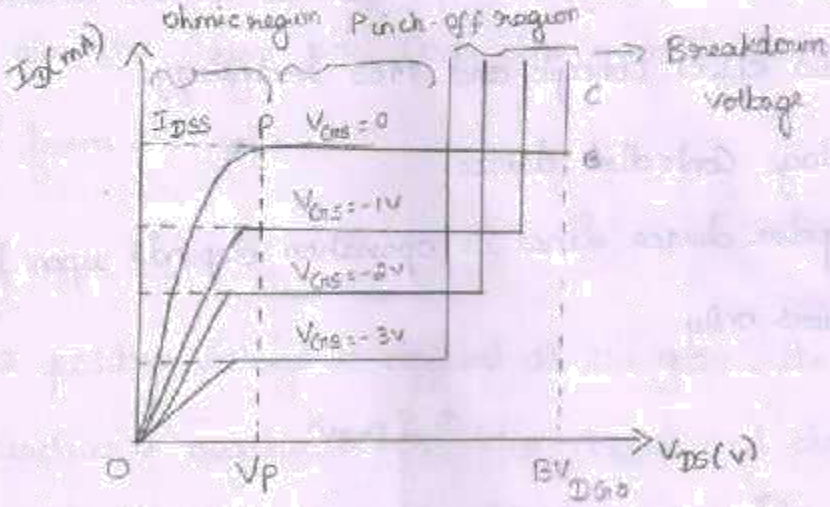
$$I_D = \frac{V_{DS}}{R} = \frac{AV_{DS}}{\rho L}$$

$$\therefore R = \frac{\rho L}{A}$$

→ Due to the applied voltage $V_{DS}$ and the resistance of the channel, there is a positive potential along the channel therefore the channel across the PN junction will increase and also the

for the wedge shape of the channel.

Characteristics:




→ When $V_{DS}$ is increased, the cross sectional area of the channel will get reduced

→ At certain value of ($V_p$) of $V_{DS}$, the area at B becomes maximum. At this voltage the channel is said to be pinched off and the voltage $V_p$ is called **pinch off voltage**

→ The above characteristics has three region

Ohmic region
Pinch off region
Breakdown voltage region.

→ when $V_{DS}$ increased from zero, $I_D$ will increase along OP and the rate of increase of $I_D$ with $V_{DS}$ decreased.

→ The region from $V_{DS}=0V$ to $V_{DS}=V_p$ is called ohmic region.

→ when $V_{DS}=V_p$ $I_D$ will be maximum and when $V_{DS}$ increased beyond $V_p$, the length of the saturation region will increase

→ At certain voltage, $I_D$ will decrease suddenly and this is due to the avalanche multiplication of electrons.

→ The drain voltage at which the breakdown occurs is denoted by $BV_{DSO}$

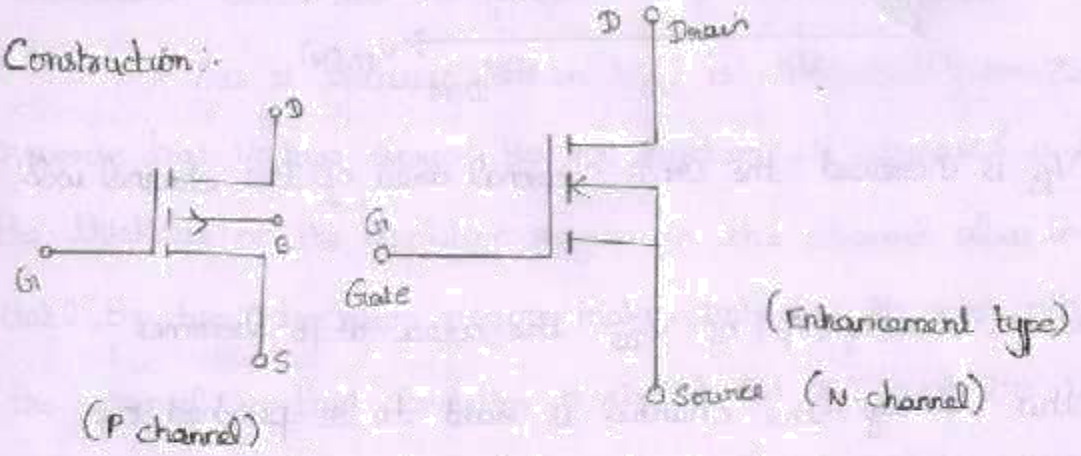
MOSFET :-

→ It is a recently developed device which combines the areas of field effect concept and MOS technology.

→ Voltage Controlled device

→ Unipolar device since its operation depends upon flow of majority carriers only

Construction :-

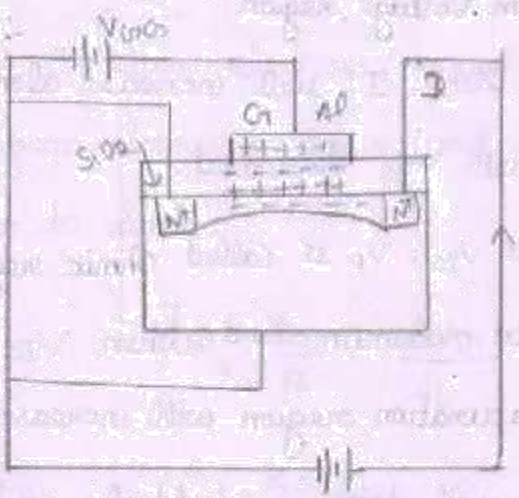



⇒ There are two basic forms

Enhancement MOSFET

Depletion MOSFET

Construction :-




→ Two highly doped $N^+$ regions are diffused in a lightly doped substrate of P type silicon substrate.

→ One $N^+$ region is source and other is Drain & substrate is connected by $10^{-3}$ cm

→ A thin insulating layer of $SiO_2$ is grown over the surface and over this $SiO_2$ layer, a thin layer of aluminium is formed. and also this layer will cover the overall channel region and it will form the gate G.

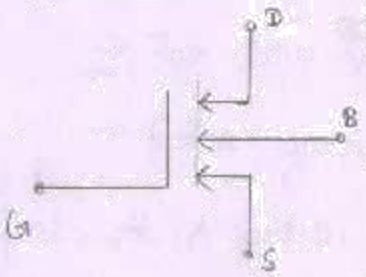
Operation:-

→ If a positive voltage is applied at the gate, the positive charge will induce a negative charge b/w Source and drain and as a result, an electric field is produced b/w Source and drain.

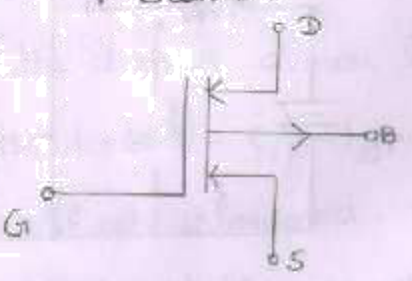
→ When the +ve voltage on gate increases, the induced negative charge in the semiconductor will increase and hence the conductivity increases and current will flow from Source to drain.

Depletion MOSFET

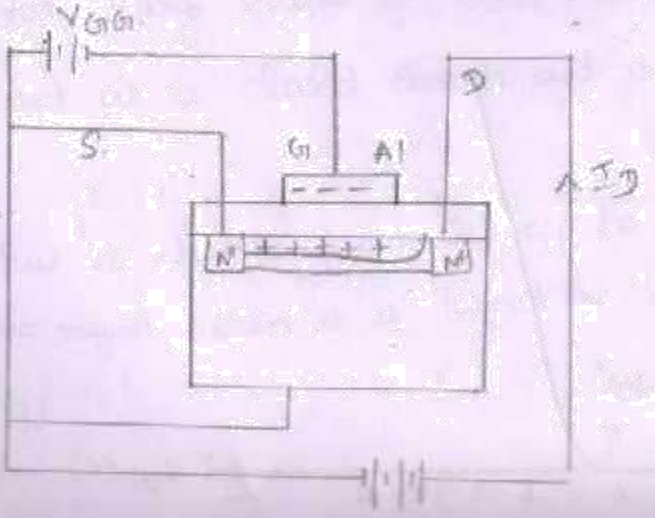
N-channel:-




P channel:-




Construction:



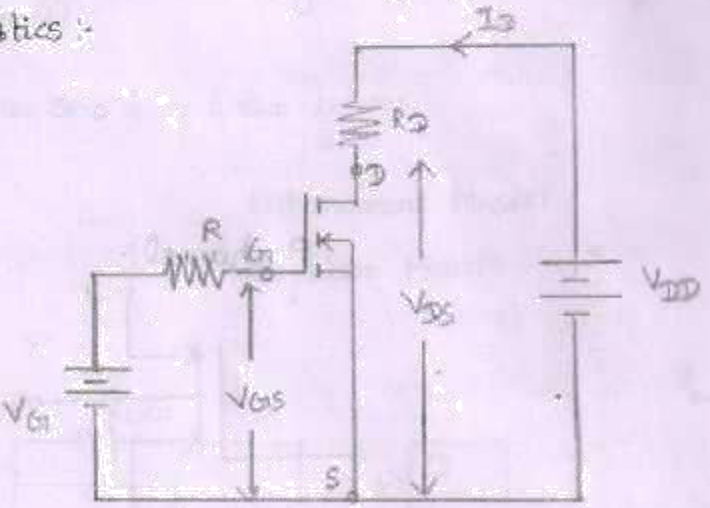
→ N-channel is diffused between the Source and drain and the remaining Construction is similar to the enhancement Mosfet.

Operation :

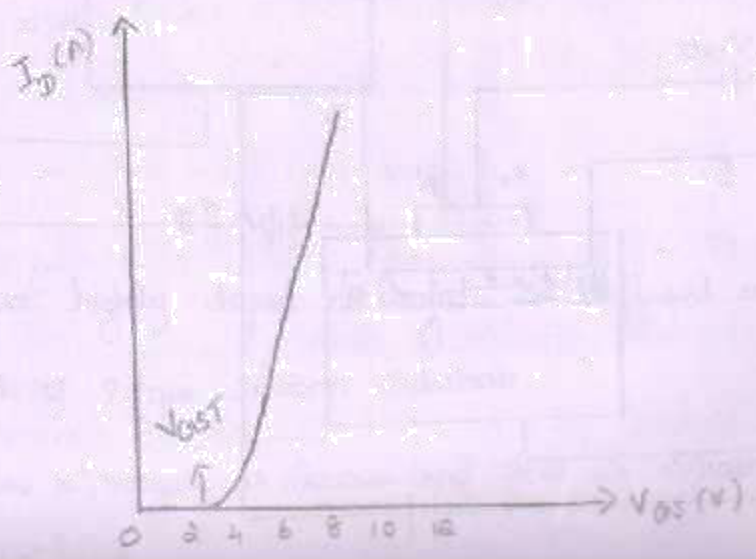
→ when D is at positive potential with respect to Source, the electrons will flow from S to D through N channel, and as a result $I_D$ will flow through D to S.

→ If the gate voltage is made negative, the positive charge will induced which will cause the depletion of mobile electrons and hence a depletion region is produced and its shape will depend upon $V_{GS}$ and $V_{DS}$.

Characteristics :-




Transfer characteristics

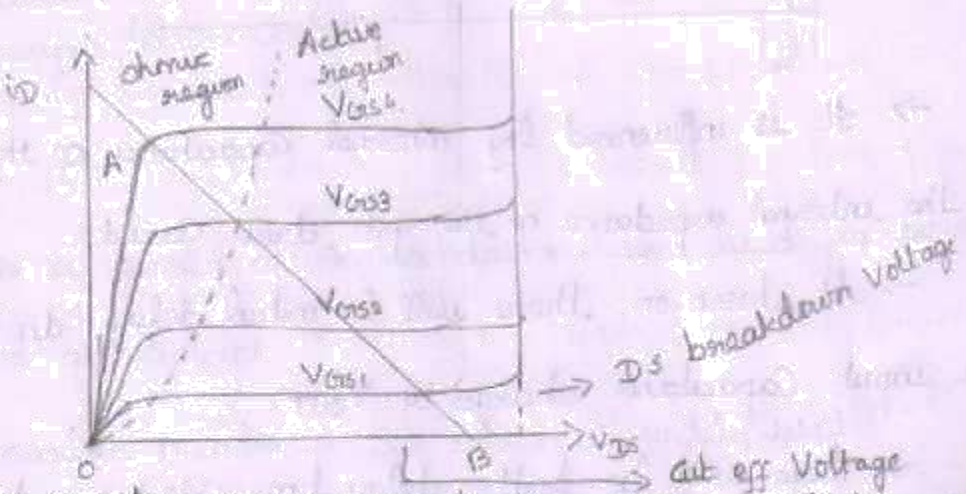


→ It shows the variation of drain current as a function of gate source voltage.

→ $V_{GS(T)}$ is the minimum positive voltage between gate and source to induce N channel. It is in the order of 2 to 3 V.

→ For a threshold voltage below $V_{GS(T)}$, device will be in off state.

Output characteristics:




→ The variation of $I_D$ as a function of $V_{DS}$, with $V_{GS}$ as a parameter will give the output characteristics.

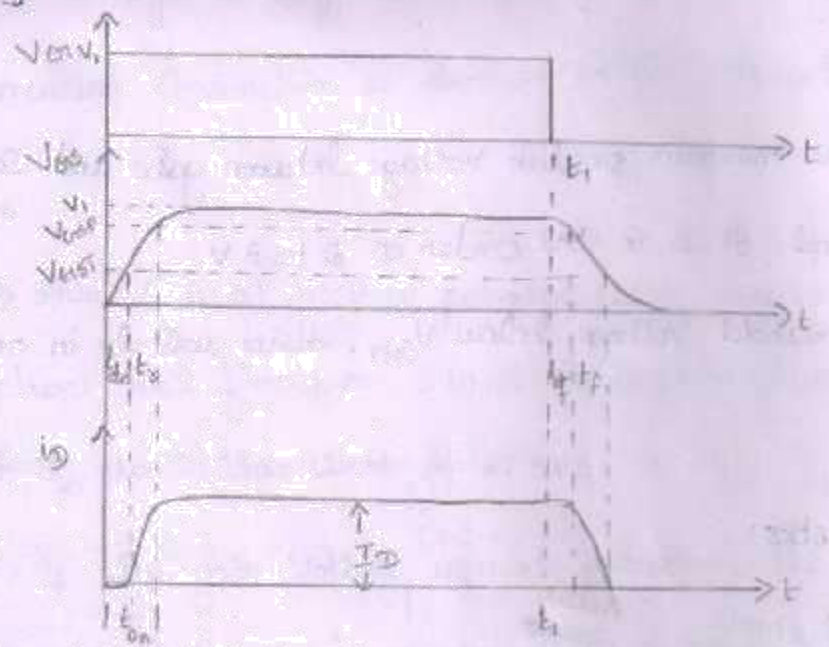
→ For low values of $V_{DS}$, the char is almost linear.

→ For a given $V_{GS}$, if $V_{DS}$ is increased, O/p characteristics is flat. At A and B, a load line will get intersected. A indicates a fully on condition and B indicates a fully off state.

→ For large values of $V_{GS}$, MOSFET will turned ON and it will act as a closed switch and it will reach ohmic region.

→ Thus it changes from cut off to active region and then to ohmic region when it is turned on and vice versa when it is turned off.

Switching characteristics:




→ $t_f$ is influenced by internal capacitance of the device and the internal impedance of the gate drive circuit.

→ At turn on, there will be initial delay $t_{dn}$ during which input capacitance charges to $V_{GST}$.

→ There will be further delay time called rise time during which gate voltage rises to $V_{GSP}$ used to turn on the MOSFET

→ The total turn on time is given by,

$$t_{on} = t_{dn} + t_s$$

→ As soon as the removal of gate voltage at time $t_1$, turn-off process will be initiated.

→ $t_{df}$ is the time during which input capacitance discharges from $V_1$ to $V_{GSP}$.

→ $t_f$ is the time during which input capacitance discharge from $V_{GSP}$ to threshold voltage.

→ when $V_{GS} \leq V_{GST}$, MOSFET will be turned off.

Advantage:

→ High input impedance
→ Lower Switching losses
→ Has positive temperature coefficient.
→ Absence of Secondary breakdown.

Application:

→ Induction heating
→ Robotics
→ Steppes motor Control.

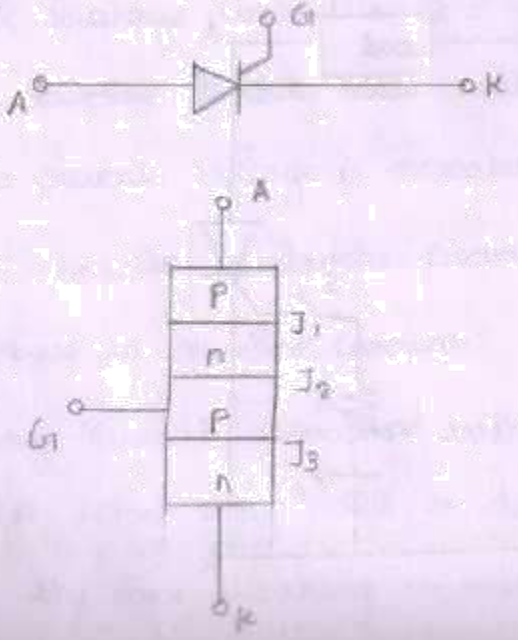
Thyristor:

→ Denotes a family of semiconductor devices used for power control in dc and ac systems.

→ The earliest member is SCR which is widely used.

→ It is derived from the combination of THYRATRON and TRANSISTOR because it is a solid state device like transistor and has characteristics similar to thyratron tube.

Construction:



→ It is a four layer three junction p n p n semiconductor switching device

→ It has three terminals

Anode
Cathode
Gate

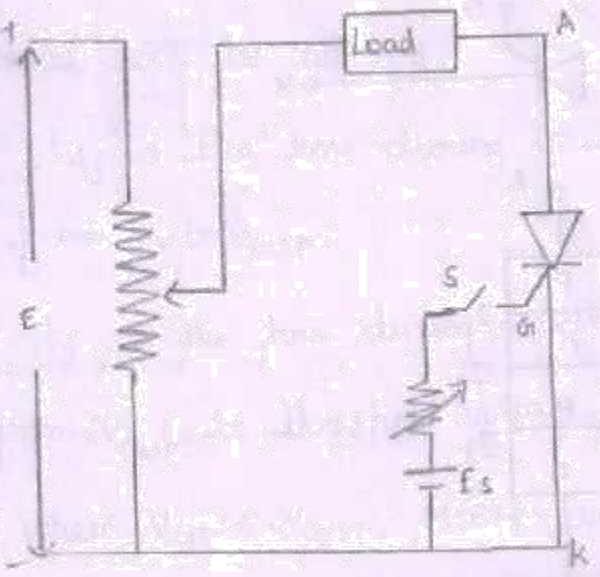
→ Normally, it consist of four layers of alternate P type and n type Silicon semiconductors forming three junction $J_1, J_2, J_3$.

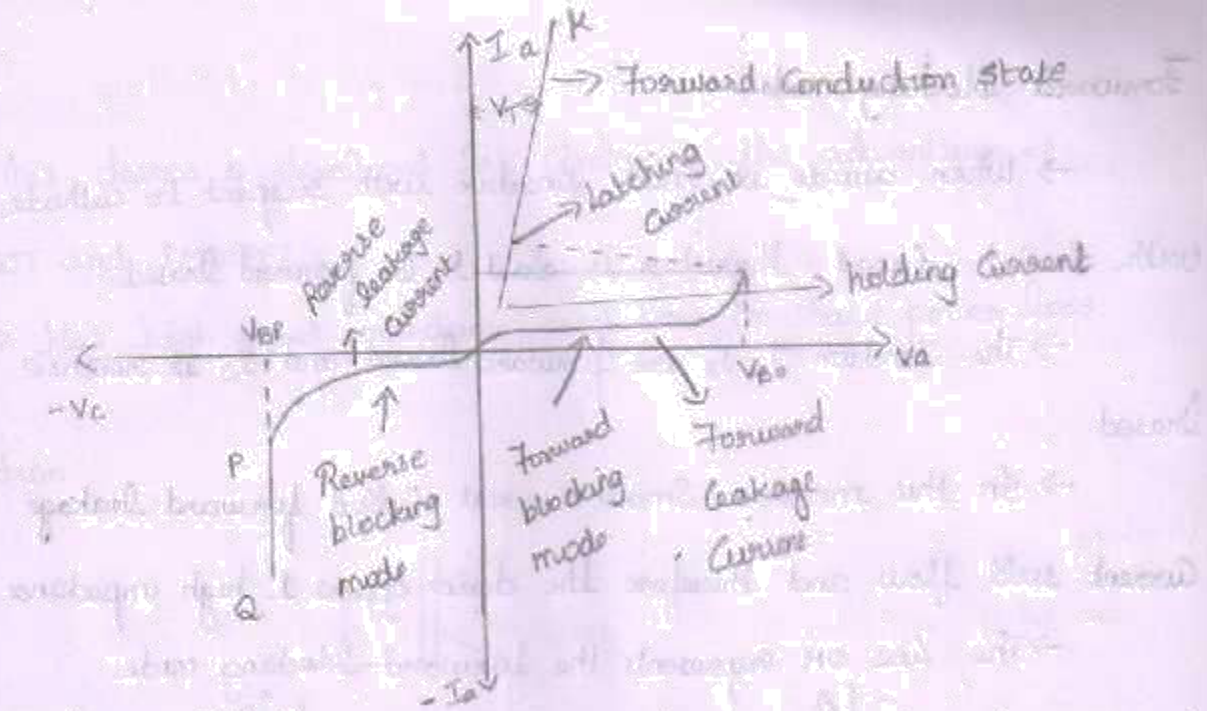
→ For tightening the thyristor to the heat sink with a help of a nut, a threaded portion is needed.

→ The terminal connected to outer P region is called anode and terminal connected to outer n region is called Cathode and that connected to inner P region is called Gate.

→ When the thyristor is used for large current rating, thyristor need better cooling and it can be achieved by mounting them on heat sinks.

Characteristics :






→ It has three basic modes of operation

Reverse Blocking mode

Forward Blocking mode

Forward Conduction mode

Reverse Blocking mode:

→ When Cathode is made positive with respect to anode with Switch S open, the thyristor is reverse biased

→ Junctions $J_1$, $J_3$ are reverse biased and $J_2$ is forward biased

→ A small leakage Current of the order of few mA will flow. This is the reverse blocking mode indicated by OP.

→ If the reverse voltage is increased, then at reverse breakdown voltage $V_{BR}$, an avalanche occurs at $J_1$ and $J_3$ and there is rapid increase in reverse Current.

→ A large Current associated with $V_{BR}$ give rise to more losses in SCR which may result in damage to the thyristor. Therefore the max withstanding reverse voltage should does not

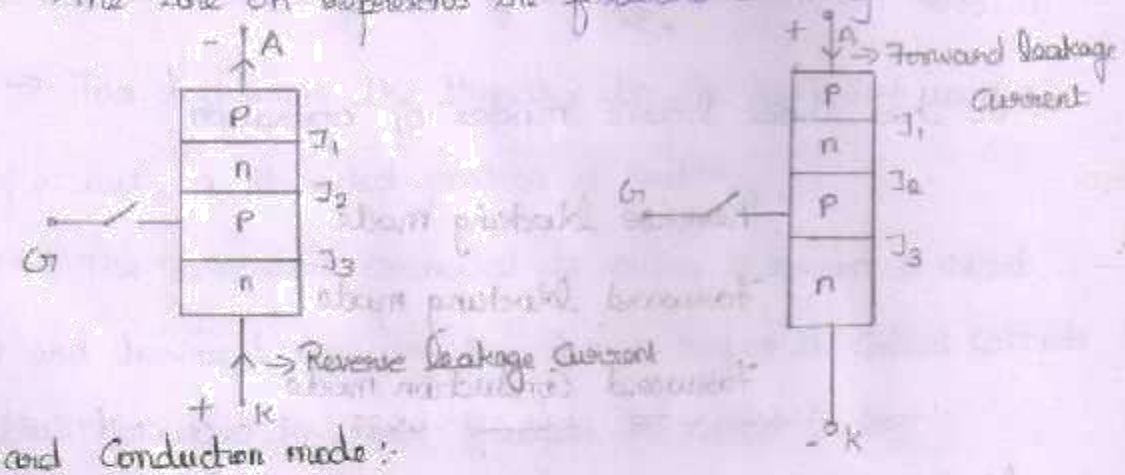
Forward Blocking mode:

→ When anode is made positive with respect to cathode, with Switch closed, thyristor is said to be forward biased.

→ The Junction $J_1$, $J_3$ are forward biased and $J_2$ is reverse biased

→ In this mode a small current called forward leakage current will flow and therefore the device offers a high impedance.

→ The line OH represents the forward blocking mode.




Forward Conduction mode:-

→ When anode to cathode forward voltage is increased with gate circuit open, reverse biased junction $J_2$ will have an avalanche breakdown at a voltage called forward breakover voltage ($V_{BO}$)

→ After this breakdown, the device will get turned on with point M at once shifting to N and then to a point anywhere between N and K.

→ The region NJK represents the forward conduction mode.

→ A thyristor can be brought from forward blocking mode to forward conduction mode by turning it on by applying

i) positive gate pulse between gate and cathode

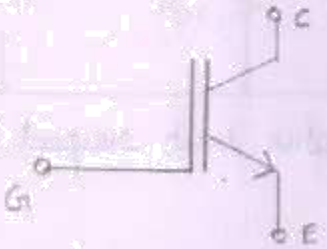
ii) a forward breakover voltage across anode & cathode.

IGBT:

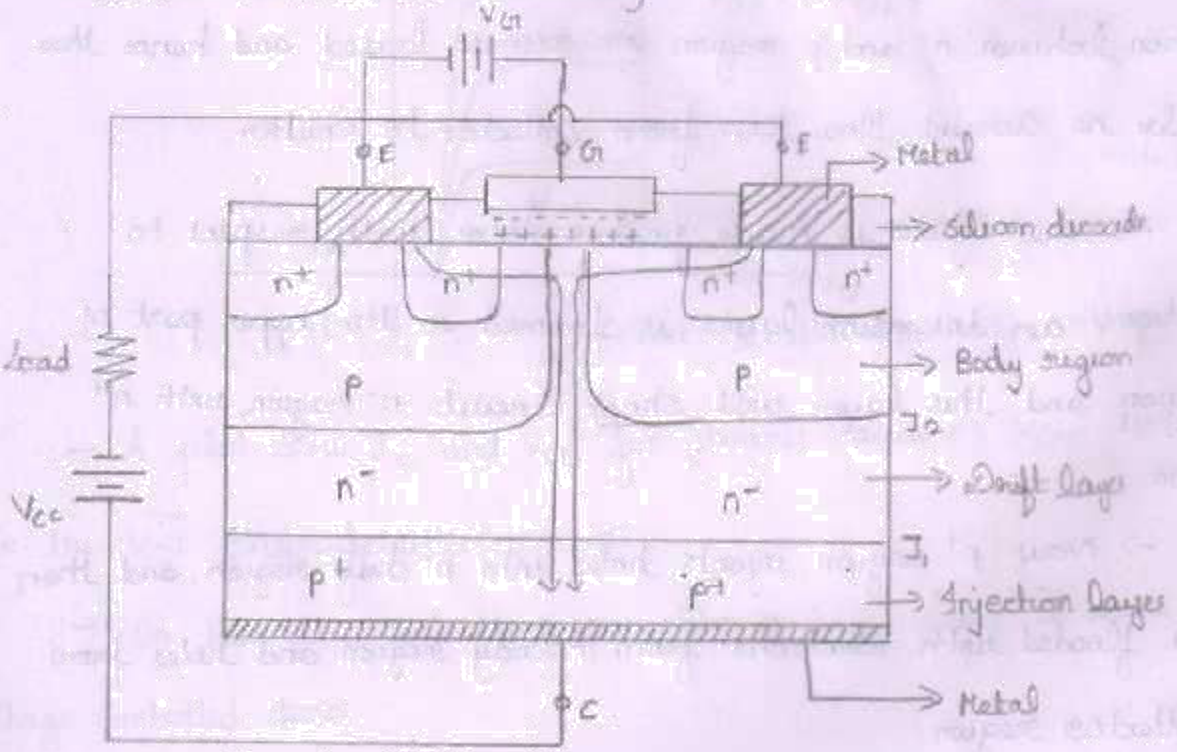
→ This device is developed by combining the advantage of both BJT and PMOSFET

→ Has high input impedance and low on-state power loss

Construction:




→ It has three terminals namely Gate, Collector and Emitter




→ On p substrate, two heavily doped $n^+$ regions are diffused

→ An insulating layer of $SiO_2$ is grown on the surface

→ Now the insulating layer is etched in order to embed metallic source and drain terminals

→ $n^+$ regions make contact with Gate and Collector terminals

→ $p^+$ substrate is called injection layer since it injects holes into $n^-$ layer. The $n^-$ layer is called drift region.

→ The thickness of the $n^-$ layer determines the voltage blocking capability of IGBT

→ The P layer is called body of IGBT. The $n^-$ layer in b/w $P^+$ and P regions serves to accomodate the depletion layer of $Pn^-$ junction

Working :-

→ when collector is made positive with respect to emitter, the device gets forward biased.

→ when there is no voltage between gate and emitter, the junction between n and p region are reverse biased and hence there will be no current flow b/w from collector to emitter.

→ when gate is made positive betw with respect to emitter, an inversion layer is formed in the upper part of P region and this layer will short circuit $n^-$ region with $n^+$ region

→ Now $p^+$ region injects holes into $n^-$ drift region and then it is flooded with electrons from P body region and holes from $P^+$ collector region

→ Due to the above operation, conductivity of $n^-$ region will get increased and therefore IGBT gets turned ON and begins to conduct $I_c$.

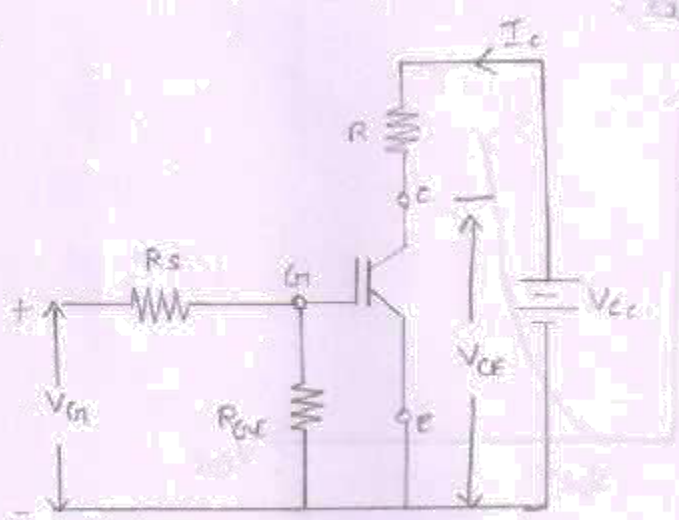
$$I_C = I_E$$

$$I_E = I_h + I_e$$

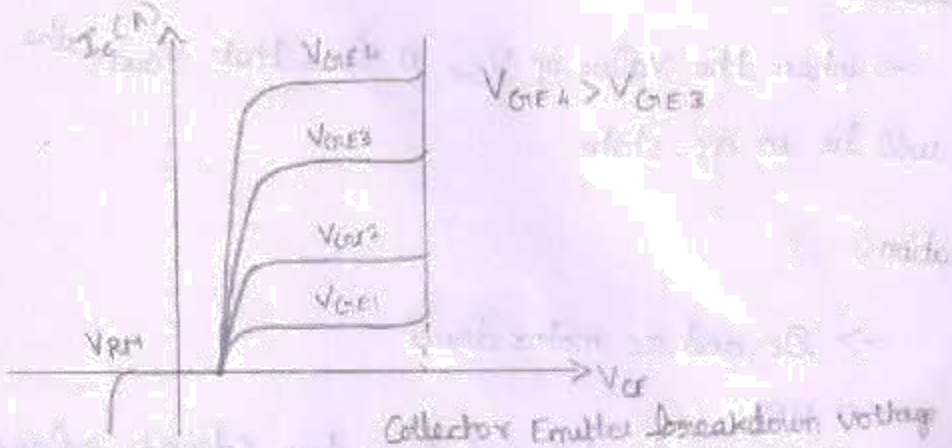
$I_h$ = hole current

$I_e$ = electron current

Characteristics:




V-I characteristics:




→ A plot b/w $I_c$ and $V_{CE}$ for various values of $V_{GE}$ will give the V-I characteristics of IGBT.

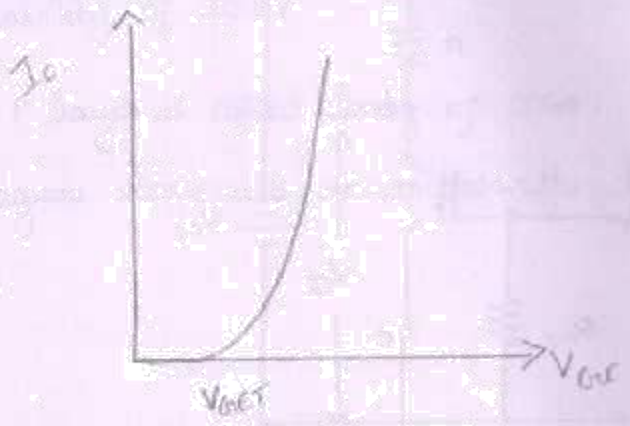
→ In this the controlling parameter is $V_{GE}$ since it is a voltage controlled device.

→ The characteristics is similar to BJT in the forward direction.

→ When the device is OFF, $J_2$ blocks forward voltage and if reverse voltage appears across collector and emitter, $J_1$ block it.

→ $V_{RM}$ is the maximum reverse breakdown voltage.

Transfer characteristics:




→ A plot b/w $I_C$ and $V_{GE}$ gives the transfer characteristics

→ when the value of $V_{GE}$ is less that $V_{GE(T)}$, the device will be in off-state

Application:

→ Dc and ac motor drives

→ UPS

→ power supplies and drives for solenoids, relays and contactors

# Unit - III - Amplifiers

## Amplifier

⇒ It is a Circuit which increases the amplitude of the given input Signal without changing the frequency

⇒ It is used in radio, television & Communication Circuits.

⇒ The amplifying elements are BJT and FET

## Classification:

a) Based on transistor Configuration

- CE amplifier
- Cc amplifier
- CB amplifier

b) Based on active device

- BJT amplifier
- FET amplifier

c) Based on operating condition

- Class A
- Class B
- Class AB
- Class C

d) Based on number of stages

- Single stage
- Multi stage

e) Based on output

- Voltage amplifier
- power amplifier

f) Based on frequency response

- Audio frequency
- Intermediate frequency
- Radio frequency

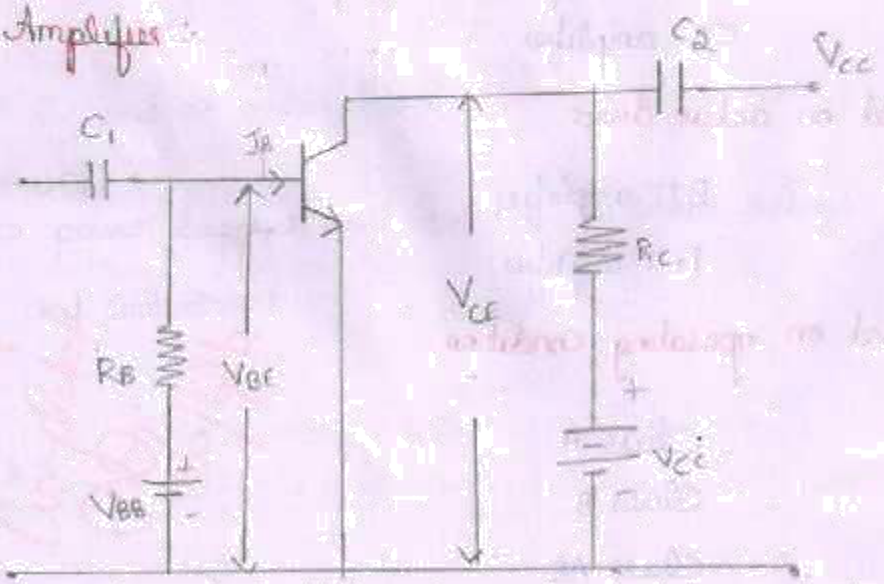
g) Based on Bandwidth

- Narrow Band
- Wide Band

Single stage Amplifier

→ It has only one amplifying device

BJT - CE Amplifier




→ The EB junction is forward biased by $V_{BB}$ and CB junction is reverse biased by $V_{cc}$ and hence the transistor remains in active region throughout the operation.

→ $C_1$, $C_2$ are the coupling capacitor to provide d.c isolation at the input and output of the amplifier

→ i/p signal is give to BE Circuit and the amplified output signal is taken from CE Circuit.

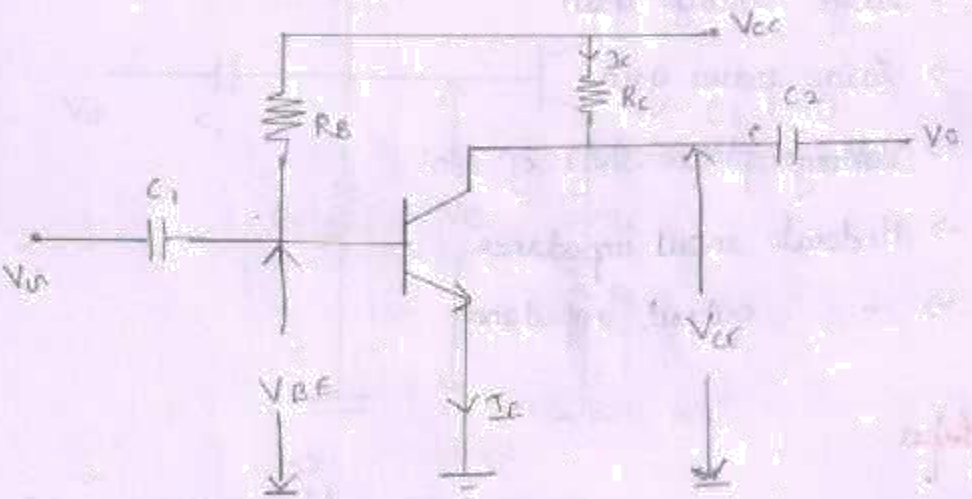
under d.c Condition

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \simeq \frac{V_{CC}}{R_B}$$

$$I_C = \beta I_B$$

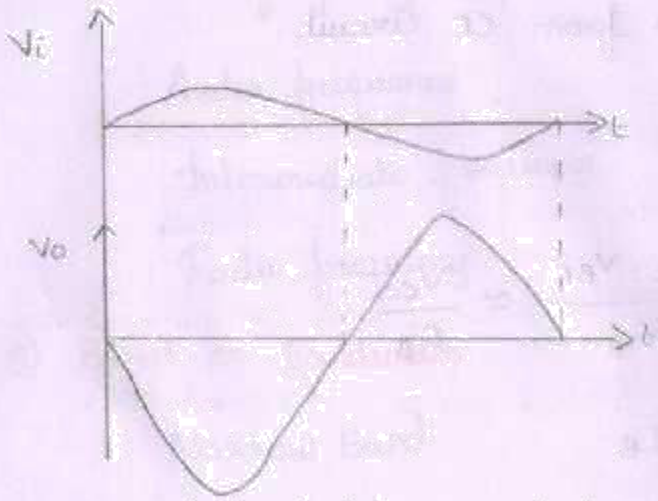
$$V_{CE} = V_{CC} - I_C R_C$$

CE Amplifier with a single power supply




→ when a.c is applied, during positive half cycle, the forward bias of the base emitter junction $V_{BE}$ is increased and hence $I_B$ will increase.

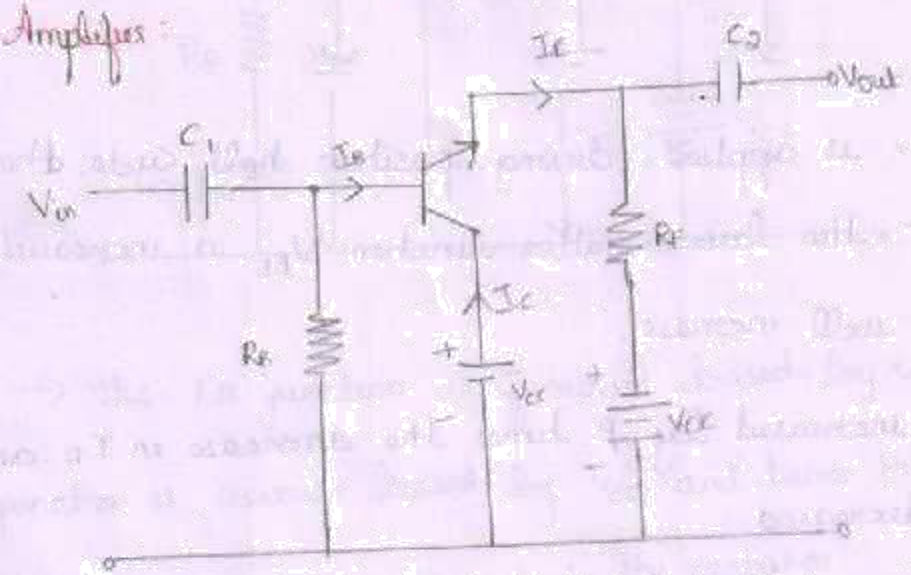
→ $I_C$ is increased by $\beta$ times the increase in $I_B$ and $V_{CE}$ will get decreased.




Characteristics:

→ Large Current gain
→ Large Voltage gain
→ Large power gain
→ Voltage phase shift of 180°
→ Moderate input impedance
→ " output impedance

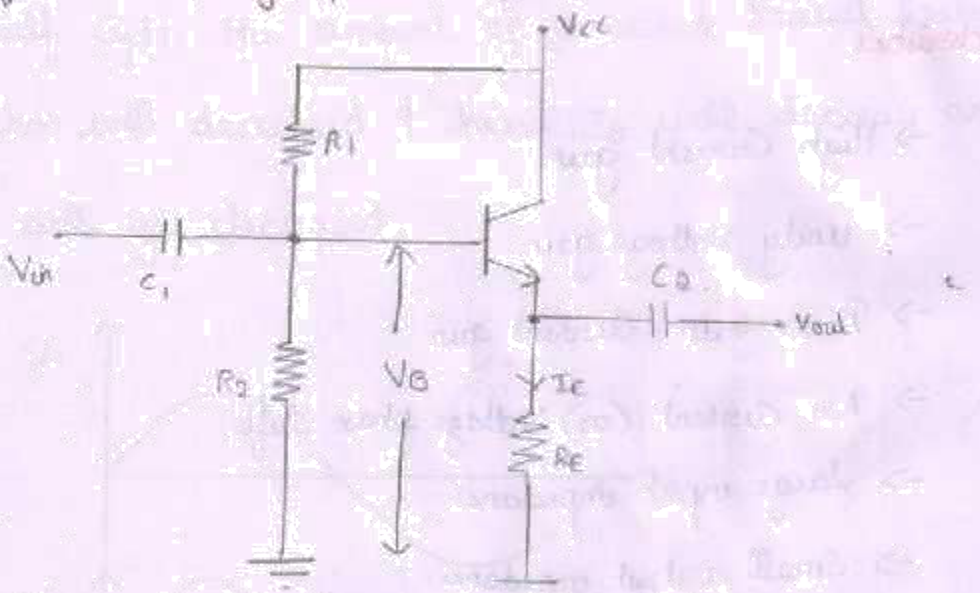
CC Amplifier:



→ The EB junction is forward biased by power supply $V_{EE}$ and CB is reverse biased by $V_{CC}$ therefore the transistor remains in the active region throughout the operation.

→ I/p signal is given to base - collector circuit and output signal is taken from emitter collector circuit.

CC Amplifier with single power supply



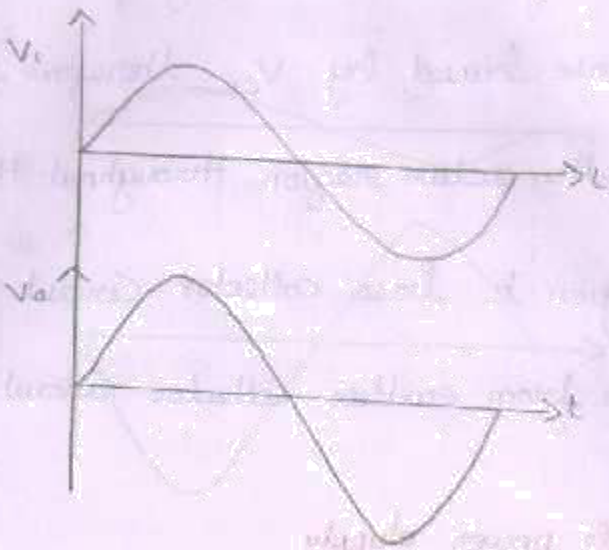

$V_0 = I_E R_E$

$V_0 = \beta I_B R_E$

→ When a.c signal is applied, during positive half cycle, $V_B$ increases and hence $I_B$ will increase.

$$I_E = I_C + I_B$$

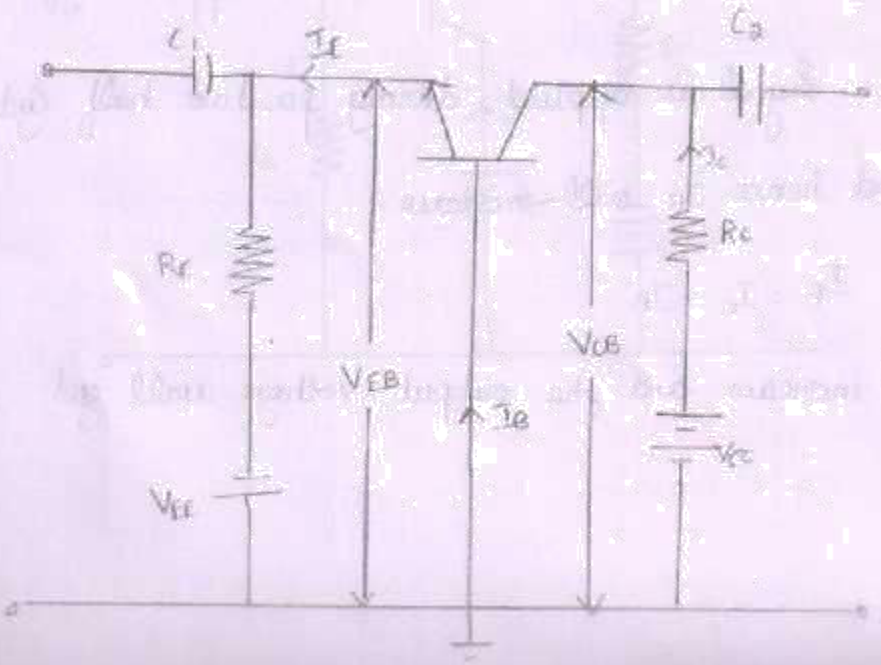
→ $I_E$ will increase and the output voltage will get increase.




Characteristics :

- → High Current gain
- → Unity Voltage gain
- → Power gain = Current gain
- → No Current (or) Voltage phase shift
- → Large input impedance
- → Small output impedance.

CB Amplifier :

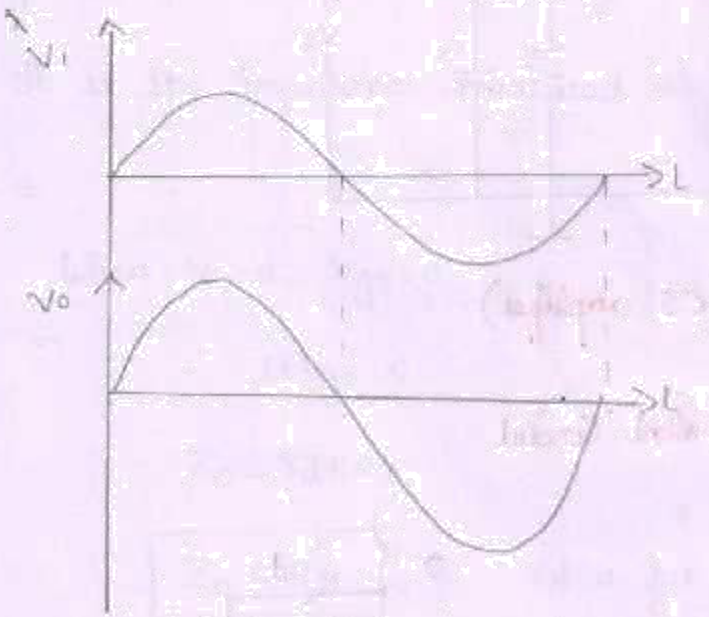


→ The EB junction is forward biased by $V_{EE}$ and CB junction is reverse biased by $V_{cc}$ and hence transistors remains in the active region throughout the operation

→ I/p signal is given to emitter base circuit and O/p signal is taken from collector base circuit

$$V_o = V_{cc} - I_c R_c$$

→ When a.c signal is applied at the input, during positive half cycle, the amount of forward biased base to BE junction will decreased & hence $I_B$ will decrease and also $I_c$ will get decreased




Characteristics

→ Current gain less than unity
→ High voltage gain
→ Power gain = Voltage gain
→ No phase shift for current (or) voltage
→ Small input and large output impedance

FET Amplifiers:

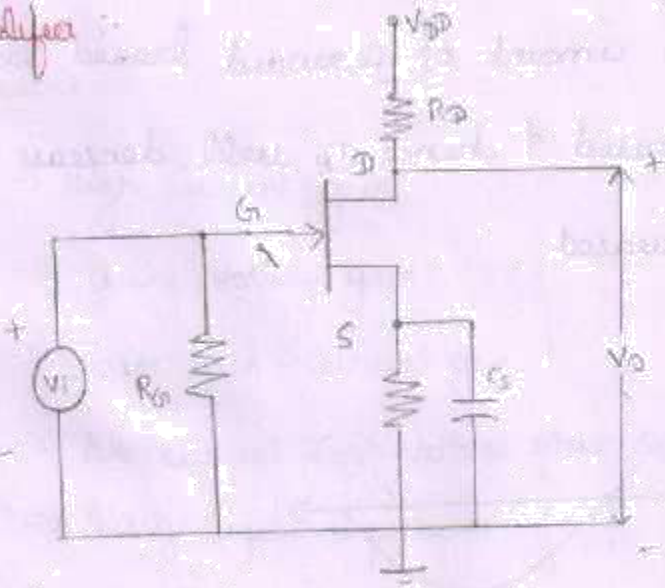
→ the Small Signal model of FET is used for analysing the FET amplifier configuration.

Common Source

Common drain (or) Source follower

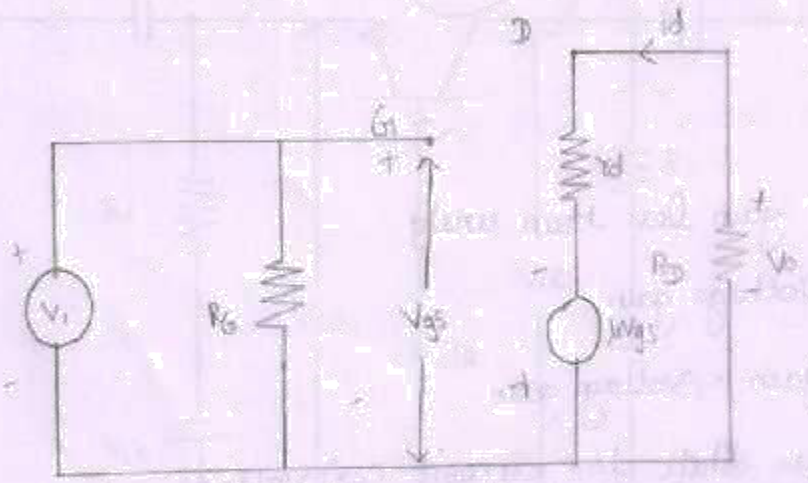
Common gate

Cs Amplifier:




(CS amplifier)

Small signal Equivalent Circuit:



Voltage gain:

$$V_o = \frac{-R_D}{R_D + r_d} \mu V_{gs}$$

$V_{gs} = V_i$ (input voltage)

Voltage gain, $A_v = \frac{V_o}{V_i} = -\frac{\mu R_D}{R_D + r_d}$

Input Impedance

$Z_i = R_G$

$R_G = R_1 \| R_2$

Output Impedance

→ It is the impedance measured at the output terminals with $V_i = 0$.

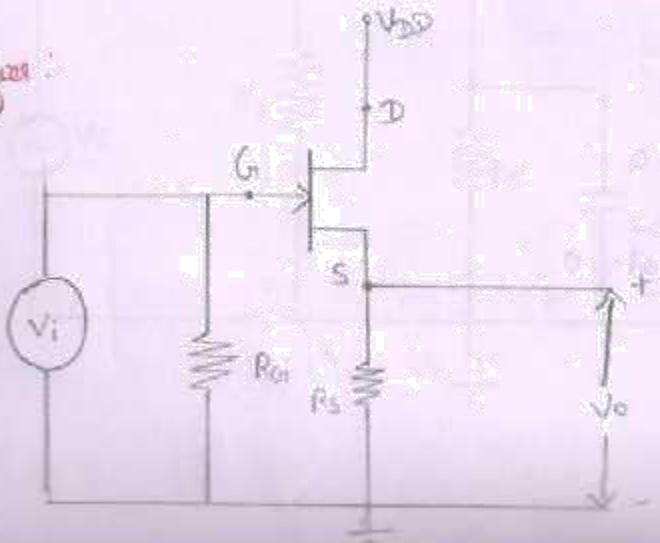
When $V_i = 0$, $V_{gs} = 0$

$\therefore \mu V_{gs} = 0$

$Z_o = r_d \| R_D$

$\boxed{Z_o \simeq R_D}$ — $r_d$ is far greater than $R_D$

CD Amplifier:



Output Impedance. $Z_o = \frac{r_d}{\mu+1} \parallel R_s$.

If $\mu >> 1$.

$$Z_o = \frac{r_d}{\mu} \parallel R_s$$

$$= \frac{1}{g_m} \parallel R_s$$

Frequency Response

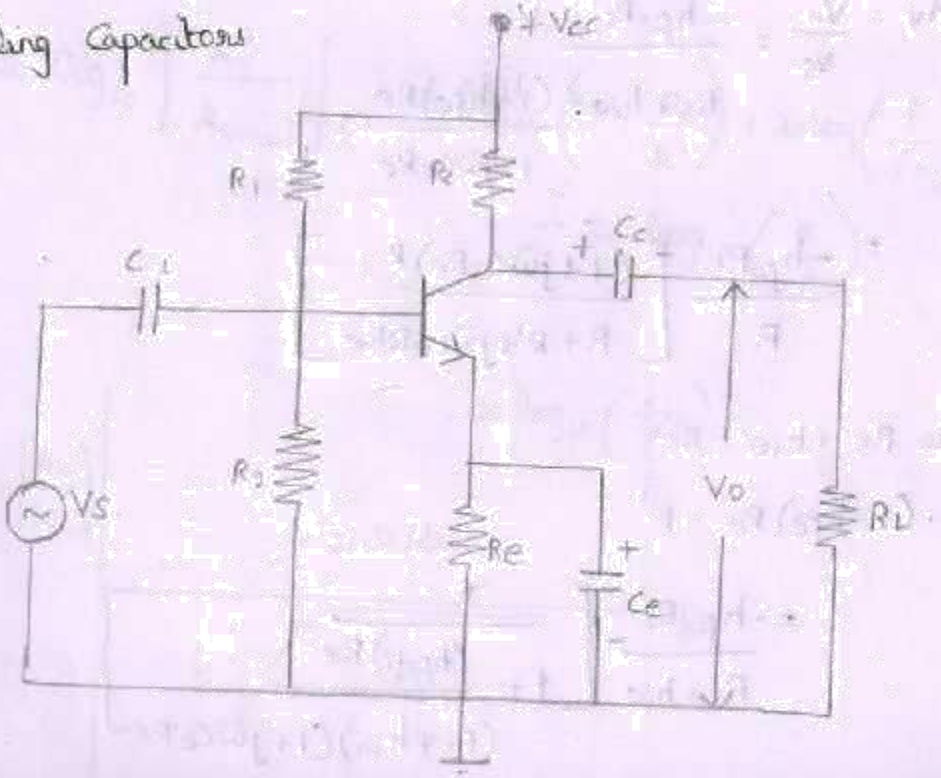
→ Defined as the measure of output parameter Variation with respect to Variation of input frequency.

→ The ratio of amplitude of the output sinusoidal to the amplitude of input sinusoidal is defined as amplifier gain.

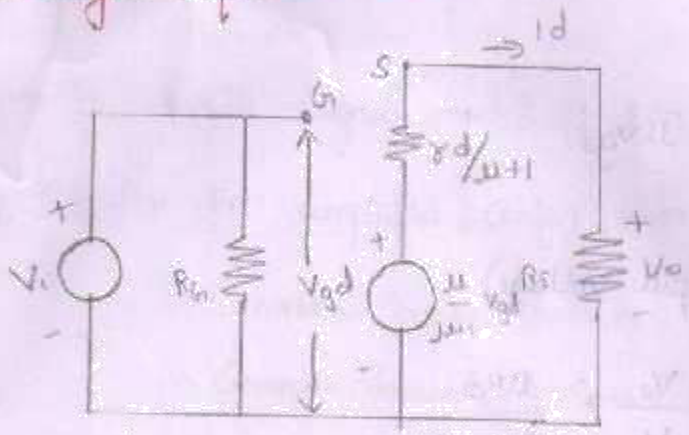
Low frequency response of BJT Amplifiers.

→ It is determined by the emitter bypass capacitor and the coupling capacitors

→



Small signal equivalent Circuit




Output Voltage $V_o = \frac{R_S}{R_S + \frac{r_d}{\mu+1}} \times \frac{\mu}{\mu+1} V_{gd}$

$$V_o = \frac{\mu R_S V_{gd}}{(\mu+1) R_S + r_d}$$

$V_{gd} = V_i$

Voltage gain

$$A_V = \frac{V_o}{V_i} = \frac{\mu R_S}{(\mu+1) R_S + r_d}$$

Input Impedance

$$Z_i = R_G$$

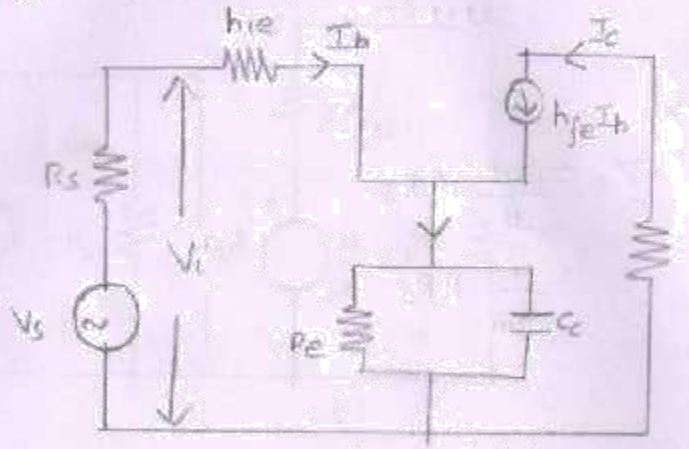
Output Impedance

→ $V_i = 0$

$V_{gd} = 0$

$\frac{\mu}{\mu+1} V_{gd} = 0$

Small signal hybrid equivalent Circuit




$$V_o = -h_{fe} I_b R_c'$$

$$I_b = \frac{V_s}{R_s + R_i}$$

$$Z_e = \frac{R_e}{1 + j\omega C_e R_e}$$

$$V_o = \frac{-h_{fe} R_c' V_s}{R_s + h_{ie} + (1 + h_{fe}) Z_e} = \frac{-h_{fe} R_c' V_s}{R_s + h_{ie} + \frac{(1 + h_{fe}) R_e}{1 + j\omega C_e R_e}}$$

$$A_v = \frac{V_o}{V_s} = \frac{-h_{fe} R_c'}{R_s + h_{ie} + \frac{(1 + h_{fe}) R_e}{1 + j\omega C_e R_e}}$$

$$= \frac{-h_{fe} R_c'}{R} \left[ \frac{(1 + j\omega C_e R_e) R}{R + R' + j\omega C_e R R_e} \right]$$

where $R_s + h_{ie} = R$

$$(1 + h_{fe}) R_e = R'$$

$$= \frac{-h_{fe} R_c'}{R_s + h_{ie}} \left[ \frac{1}{1 + \frac{(h_{fe} + 1) R_e}{(R_s + h_{ie})(1 + j\omega C_e R_e}} \right]$$

$$A_V = \frac{-h_{fe} R_c}{R_s + h_{ie}} \left[ \frac{1 + j\omega C_e R_e}{1 + j\omega C_e R_e + \frac{(1+h_{fe}) R_e}{R_s + h_{ie}}} \right]$$

$$A_V = \frac{-h_{fe} R_c}{R\left(1 + \frac{R'}{R}\right)} \left[ \frac{1 + j\omega C_e R_e}{1 + \frac{j\omega C_e R_e R}{R + R'}} \right]$$

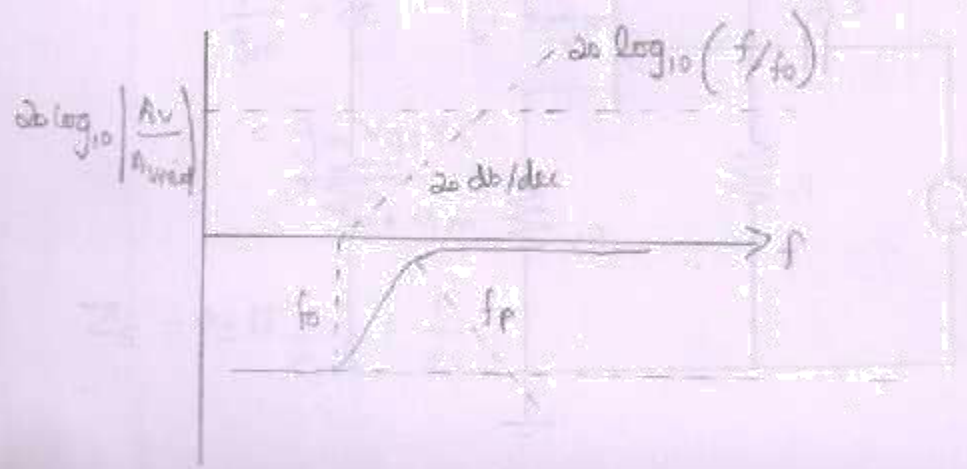
$$A_{vmid} = \frac{-h_{fe} R_c}{R}$$

$$A_V = \left[ \frac{A_{vmid}}{1 + R'/R} \right] \left[ \frac{1 + j(f/f_o)}{1 + j(f/f_p)} \right]$$

where $f_o = \frac{1}{2\pi C_e R_e}$ , $f_p = \left(\frac{R + R'}{2\pi C_e R_e R}\right) \frac{1 + \left(\frac{R'}{R}\right)}{2\pi C_e R_e}$

Gain in db,

$$20 \log_{10} \left| \frac{A_V}{A_{vmid}} \right| = 20 \log_{10} \left(1 + \frac{R}{R'}\right) + 20 \log \left(\frac{f}{f_o}\right) - 20 \log_{10} \left(\frac{f}{f_p}\right)$$



$$\frac{R'}{R} >> 1 \quad \& \quad f_p >> f_o \quad \text{at} \quad f = f_p$$

$$\left| \frac{A_v}{A_{vmid}} \right| = \frac{1}{1+\left(\frac{R'}{R}\right)} \frac{f_p/f_o}{\sqrt{1+1}} = \frac{1}{\sqrt{2}} \left(\frac{f}{f_p}\right)$$

$$f_1 = f_p \simeq \frac{(1+h_{fe})}{(R_s+h_{ie})2\pi C_e}$$

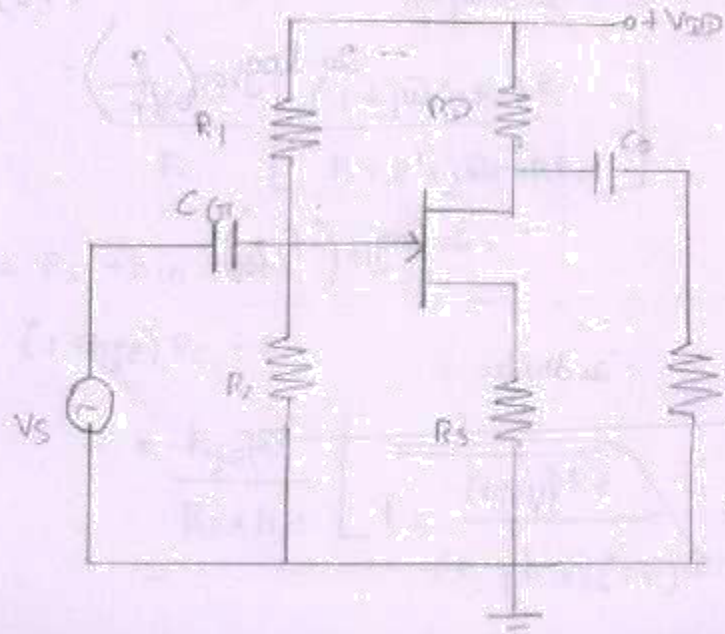
Effect of Coupling Capacitor

$$\frac{1}{\omega C_{in}} = R_i + R_s$$

$$\omega = \frac{1}{C_{in}(R_s+R_i)}$$

$$\boxed{f_1 = \frac{1}{2\pi C_{in}(R_s+R_i)}}$$

Low frequency response of JFET amplifier:



$$V_{gs} = \frac{V_s R_{G1}}{R_{G1} + R + \frac{1}{sC_{G1}}}$$

$$= \frac{V_s R_{G1} \cdot s}{(R_{G1}+R)\, s + \frac{1}{C_{G1}}}$$

$$V_{gs} = \frac{V_s R_{G1}}{R_{G1}+R} \left[ \frac{s}{s + \frac{1}{C_{G1}(R_{G1}+R)}} \right]$$

$$\frac{V_{gs}}{V_s} = \frac{R_{G1}}{R_{G1}+R} \times \left[ \frac{s}{s + \frac{1}{C_{G1}(R_{G1}+R)}} \right]$$

$$= \frac{R_{G1}}{R_{G1}+R} \left[ \frac{s}{s + 1/\tau} \right]$$

$$\omega_{P1} = \frac{1}{C_{G1}(R_{G1}+R)} = 1/\tau$$

Effect of bypass Capacitor :

$$I_d = \frac{V_{gs}}{\frac{1}{g_m} + Z_S} = \frac{g_m V_{gs}}{1 + Z_S g_m}$$

$$= \frac{g_m V_{gs} Y_S}{Y_S + g_m}$$

$$Z_S = R_S \,||\, \frac{1}{C_S s} = \frac{1}{Y_S}$$

$$I_d = \frac{g_m \left(\frac{1}{R_S} + sC_S\right) V_{gs}}{\frac{1}{R_S} + sC_S + g_m}$$

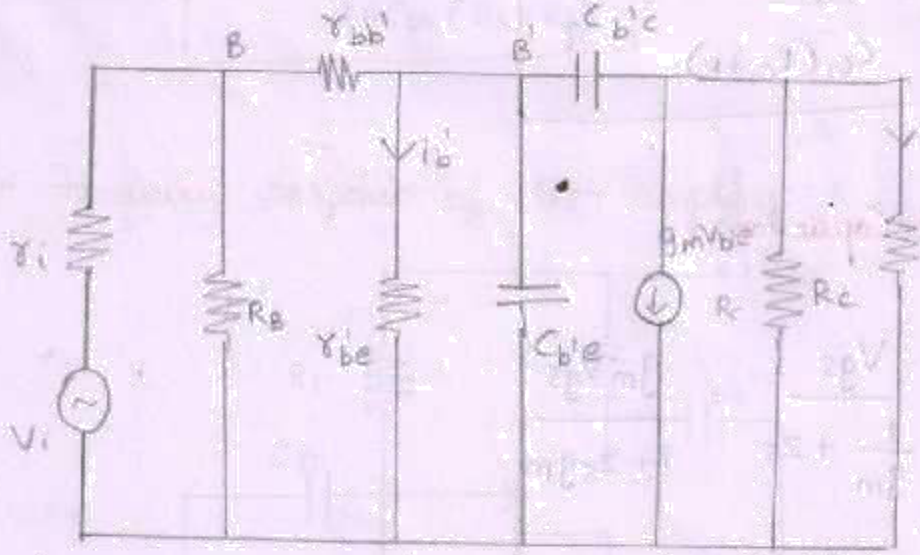
$$I_d = \frac{g_m V_{gs} \left(s + \frac{1}{R_S C_S}\right)}{s + \left(\frac{1}{R_S} + g_m\right)\frac{1}{C_S}}$$

$$\omega_{P2} = \frac{1}{C_S}\left(\frac{1}{R_S} + g_m\right)$$

$$\omega_2 = \frac{1}{R_S C_S}$$

## High frequency analysis

i) BJT amplifier :



Let $r_{b'o} = h_{ie}$

$g_m V_{b'e} = h_{fe} I_b$

$$g_m = \frac{h_{fe}}{h_{ie}}$$

$$R_{b'e} = r_{b'e} \parallel (R_b + r_{b'b})$$

$$R_o = R_c \parallel R_L$$

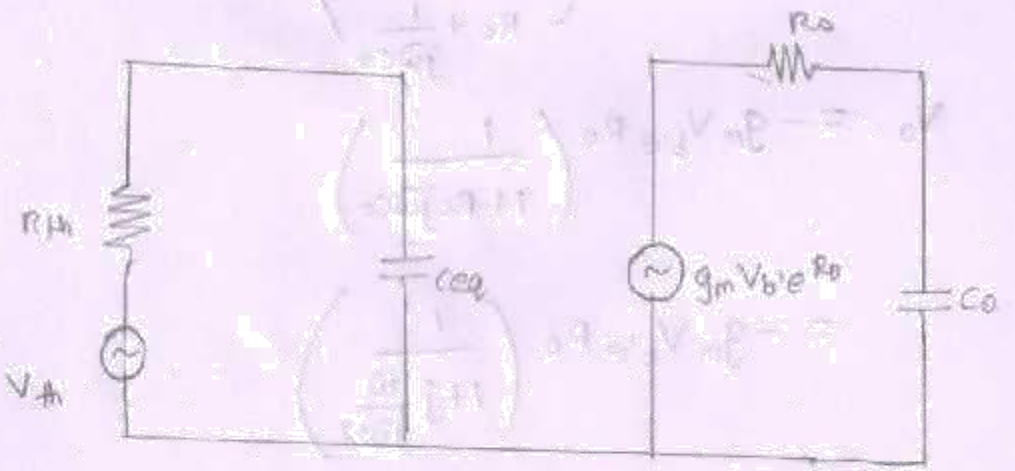
$$C_{eq} = C_{b'e} + C_{b'e}(1 + A_v)$$

$$C_{eq} = C_{b'e} + C_{b'e}(1 + g_m R_L)$$

$$C_o = \frac{C_{b'c}(1+A)}{A}$$

$$= \frac{C_{b'c}(1 + g_m R_L)}{g_m R_L}$$

$$C_o = C_{b'c}\left(1 + \frac{1}{g_m R_L}\right)$$



$$V_{th} = \frac{R_{b'e} V_s}{r_i + R'_{be}}$$

$$V_{b'e} = \left( \frac{\frac{1}{j\omega C_{eq}}}{R_{th} + \frac{1}{j\omega C_{eq}}} \right) \left( \frac{R_{b'e} \cdot V_s}{r_i + R'_{be}} \right)$$

$$V_{b'e} = \left( \frac{1}{R_{th} j\omega C_{eq} + 1} \right) \left( \frac{R_{b'e}}{r_i + R'_{be}} \right) V_s$$

$$= \frac{1}{1 + j\left(\frac{\omega}{\omega_{21}}\right)} \left( \frac{R_{b'e}}{r_i + R'_{be}} \right) V_s$$

$$\omega_{21} = \frac{1}{R_{th} C_{eq}}$$

By Considering o/p Circuit,

$$V_o = -g_m V_{b'e} R_0 \left( \frac{\frac{1}{j\omega C_0}}{R_0 + \frac{1}{j\omega C_0}} \right)$$

$$V_o = -g_m V_{b'e} R_0 \left( \frac{1}{1 + R_0 j\omega C_0} \right)$$

$$= -g_m V_{b'e} R_0 \left( \frac{1}{1 + j\frac{\omega}{\omega_{22}}} \right)$$

$$\omega_{22} = \frac{1}{R_0 C_0}$$

$$A_v = \frac{V_o}{V_s} = \frac{V_{b'e}}{V_s} \cdot \frac{V_o}{V_{b'e}}$$

$$A_v = -\frac{1}{1+j\frac{\omega}{\omega_{21}}} \left(\frac{R_{b'e}}{\gamma_i + R_{b'e}}\right) g_m \cdot R_D \left(\frac{1}{1+j\left(\frac{\omega}{\omega_{22}}\right)}\right)$$

$$A_v = A_{V01}\, V_{V02} \left(\frac{1}{1+j\frac{\omega}{\omega_{21}}}\right)\left(\frac{1}{1+j\left(\frac{\omega}{\omega_{22}}\right)}\right)$$

$$A_v = A_{Vo} \left(\frac{1}{1+j\frac{\omega}{\omega_{21}}}\right)\left(\frac{1}{1+j\left(\frac{\omega}{\omega_{22}}\right)}\right)$$

Don't Fn Completed Ray.

$$A_{V_1} = \frac{V_2}{V_1} = A_1 \angle \theta_1$$

$A_1 \rightarrow$ Voltage gain of first stage

$\theta_1 \rightarrow$ phase angle between output and input voltage of this stage.

Hence, $A_V = \frac{V_o}{V_1} = \frac{V_2}{V_1} \cdot \frac{V_3}{V_2} \cdots \frac{V_n}{V_{n-1}} \cdot \frac{V_o}{V_n}$

$$= A_{V_1} \cdot A_{V_2} \cdot A_{V_3} \cdot A_{V_4} \cdots A_{V_{n-1}} \cdot A_{V_n}$$

$$= A_1 A_2 \cdots A_n \angle \theta_1 + \theta_2 + \cdots + \theta_n$$

$$A_V = A \angle \theta$$

$\rightarrow$ The voltage gain interms of current gain.

$$A_V = \frac{A_i R_L}{R_i}$$

For $n^{th}$ stage, $A_{V_n} = \frac{A_i R_{Ln}}{R_{in}}$

$\rightarrow$ The current gain and input impedance of $n^{th}$ stage is given by.

$$A_{in} = \frac{-h_{fe}}{1 + h_{oe} R_{Ln}}$$

$$R_{in} = h_{ie} + h_{re} A_{in} R_{Ln}$$

⇒ It is important to note that which type of Connection must be used in Cascade to obtain the maximum Voltage gain and other desired characteristics.

⇒ The CC Configuration will not be used in intermediate Stage hence the Voltage gain is less than unity.

⇒ In many Cases, CC (or) CB stage is used as input because of impedance Consideration even at the expense of Voltage (or) Current gain.

Effect of Cascading of Amplifiers

⇒ when one (or) more stage Connected in the Cascade, the output of the first stage is Connected to the input of the second stage and So on, result in which there will be a significant change in the overall frequency response.

⇒ In the high frequency region, the output Capacitance $C_o$ must include the wiring Capacitance (or) stray Capacitance, the parasitic Capacitance and miller Capacitance.

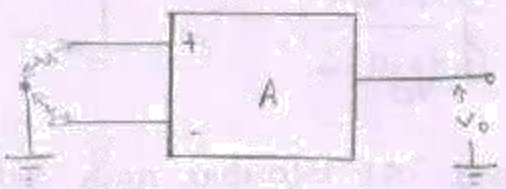
→ Further there will be additional low frequency gain levels due to the second stage having the lowest cutoff frequency. The lowest cutoff frequency is determined by the stage having the highest lower cutoff frequency.

⇒

## Differential Amplifier :-

⇒ The function of differential amplifier is to amplify the difference between two signals.

→ The need for differential amplifier arises in many physical measurements where response from d.c to many megahertz is required.



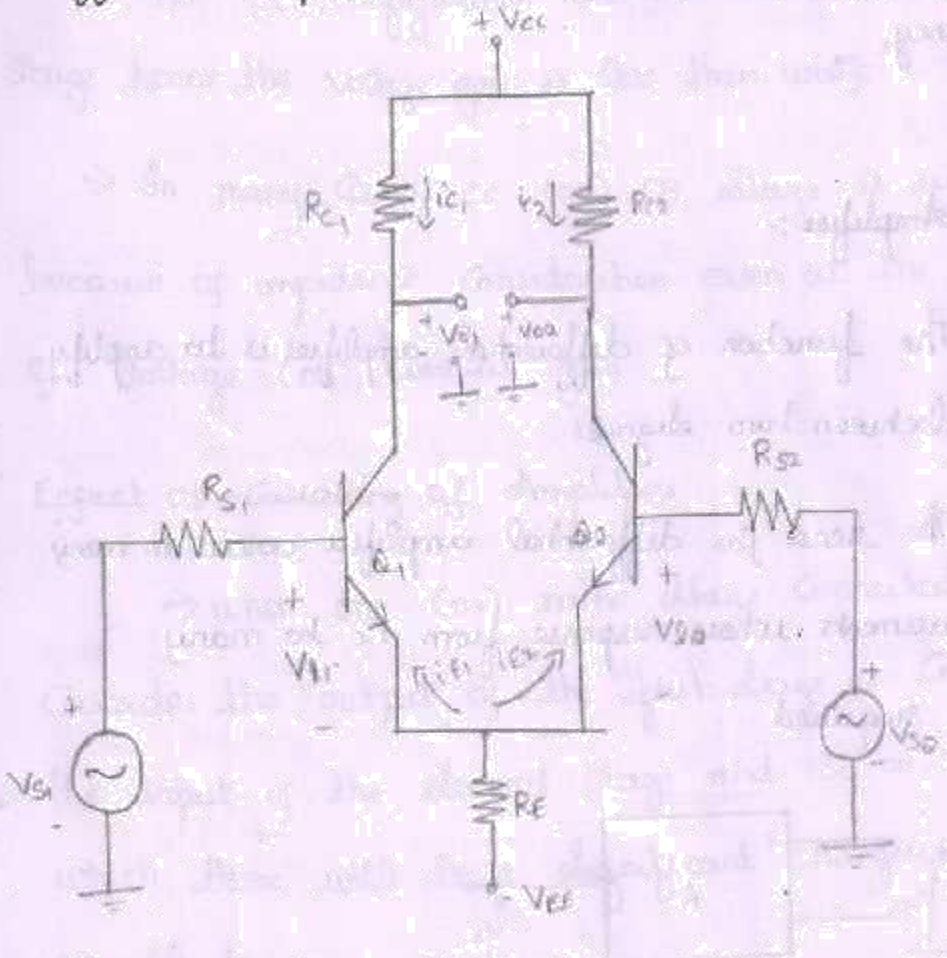

→ The output signal in a differential amplifier is proportional to the difference between the two input signal.

$$V_o = A_d (V_1 - V_2)$$

→ If $V_1 - V_2$, the output voltage is zero. A non-zero output is obtained if $V_1$ and $V_2$ are not equal.

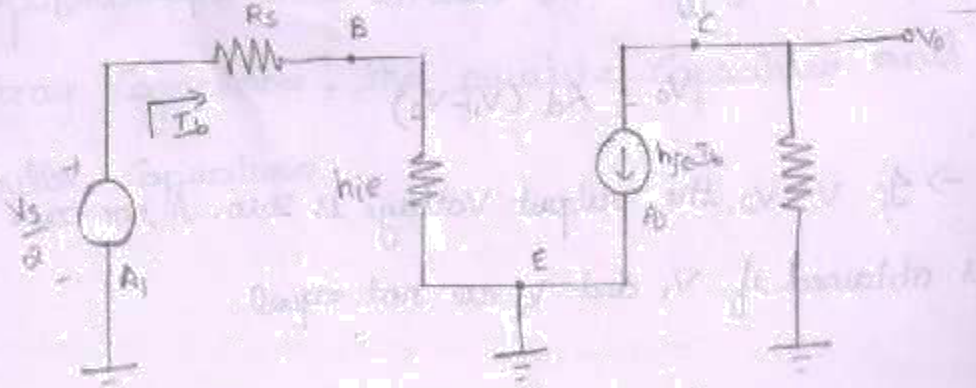
⇒ The difference mode input voltage is defined as $V_d = (V_1 - V_2)$ and the common mode input voltage is defined as $V_{cm} = \frac{(V_1 + V_2)}{2}$

Differential amplifier using BJT :-




A.c analysis

Differential mode gain:



→ Let the two signals have a magnitude of $V_s/2$ and differ from each other by 180° phase shift.

→ Since $I_{E_1} = I_{E_2}$ and out of phase by 180°, they cancel each other.

→ Applying KVL to loop $A_1$, the input loop.

$$I_b (R_s + h_{ie}) = \frac{V_s}{2}$$

$$I_b = \frac{V_s}{2(R_s + h_{ie})}$$

→ Apply KVL to loop $A_2$, the output voltage is

$$V_o = -h_{fe} I_b R_c$$

$$V_o = -h_{fe} R_c \frac{V_s}{2(R_s + h_{ie})}$$

$$\frac{V_o}{V_s} = -\frac{h_{fe} R_c}{2(R_s + h_{ie})}$$

→ Negative sign indicates 180° phase difference between input and output. As the magnitude of the input signals are equal, and are out of phase by 180°, we have,

$$V_{id} = V_1 - V_2 = \frac{V_s}{2} - \left(-\frac{V_s}{2}\right) = V_s$$

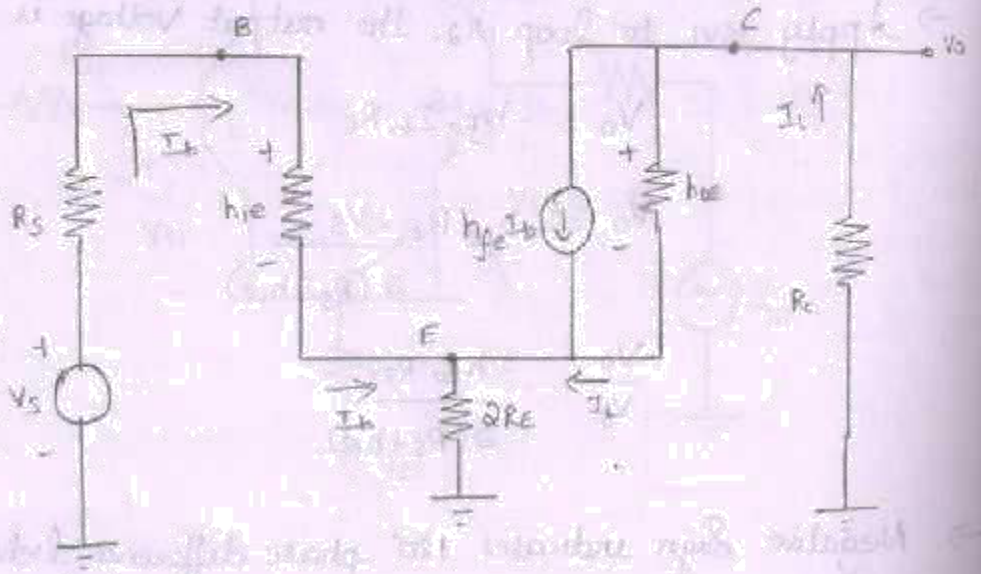
$$A_d = \frac{V_o}{V_{id}} = \frac{V_o}{V_s} = \frac{h_{fe} R_c}{2(R_s + h_{ie})}$$

⇒ When the output of a differential amplifier is measured with reference to the ground point, it is called unbalanced output.

→ $A_d$ for a balanced case can be derived by considering the balanced output across two collectors of $Q_1$ & $Q_2$.

$$A_d = \frac{2 h_{fe} R_c}{2 (R_s + h_{ie})} = \frac{h_{fe} R_c}{R_s + h_{ie}}$$

Common mode gain :-




⇒ For common mode analysis, consider that the input signals are having same magnitude $V_s$ and are in same phase. Therefore

$$V_c = \frac{V_1 + V_2}{V_2} = \frac{V_s + V_s}{2} = V_s$$

$$V_o = A_c V_c, \quad \therefore A_c = \frac{V_o}{V_s}$$

→ The Current through $R_E$ is $2I_E$. The emitter resistance is assumed to be $2R_E$ and emitter Current to be $I_E$ instead of $2I_E$.

→ Current through $R_C = I_L$

Effective emitter resistance = $2R_E$

Current through emitter resistance = $I_L + I_b$

Current through $h_{oe} = (I_L - h_{fe} I_b)$

Applying KVL to the input side,

$$I_b R_S + I_b h_{ie} + 2R_E (I_L + I_b) = V_S$$

$$V_S = I_b (R_S + h_{ie} + 2R_E) + I_L (2R_E)$$

$$V_o = -I_L R_C$$

→ Apply KVL to output loop.

$$I_L R_C + 2R_E (I_L + I_b) + \frac{(I_L - h_{fe} I_b)}{h_{oe}} = 0$$

$$I_L R_C + 2R_E I_L + 2R_E I_b + \frac{I_L}{h_{oe}} - \frac{h_{fe} I_b}{h_{oe}} = 0$$

$$I_b \left[ 2R_E - \frac{h_{fe}}{h_{oe}} \right] + I_L \left[ R_C + 2R_E + \frac{1}{h_{oe}} \right] = 0$$

$$I_L \left[ R_C + 2R_E + \frac{1}{h_{oe}} \right] = -I_b \left[ 2R_E - \frac{h_{fe}}{h_{oe}} \right]$$

$$\frac{I_L}{I_b} = \frac{\left[ \frac{h_{fe}}{h_{oe}} - 2R_E \right]}{\left[ R_C + 2R_E + \frac{1}{h_{oe}} \right]}$$

$$\frac{I_L}{I_b} = \frac{h_{fe} - 2R_E h_{oe}}{1 + h_{oe}(2R_E + R_C)}$$

$$I_b = \frac{I_L[1 + h_{oe}(2R_E + R_C)]}{h_{fe} - 2R_E h_{oe}}$$

$$V_S = \frac{I_L[1 + h_{oe}(2R_E + R_C)](R_S + h_{ie} + 2R_E)}{[h_{fe} - 2R_E h_{oe}]} + I_L 2R_E$$

$$\frac{V_S}{I_L} = \frac{[1 + h_{oe}(2R_E + R_C)](R_S + h_{ie} + 2R_E)}{h_{fe} - 2R_E h_{oe}} + 2R_E$$

$$= \frac{[1 + h_{oe}(2R_E + R_C)](R_S + h_{ie} + 2R_E) + 2R_E(h_{fe} - 2R_E h_{oe})}{h_{fe} - 2R_E h_{oe}}$$

$$\frac{V_S}{I_L} = \frac{h_{oe} R_C [R_S + h_{ie} + 2R_E] + 2R_E(1 + h_{fe}) + R_S(1 + 2R_E h_{oe}) + h_{ie}(1 + 2R_E h_{oe})}{h_{fe} - 2R_E h_{oe}}$$

Reassanging the last two terms in the numerator, we get

$$\frac{V_S}{I_L} \quad \frac{h_{oe} R_C [2R_E + R_S + h_{ie}] + 2R_E(1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_E h_{oe})}{(h_{fe} - 2R_E h_{oe})}$$

$h_{oe} R_C << 1$

$$\therefore \frac{V_S}{I_L} = \frac{2R_E(1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_E h_{oe})}{h_{fe} - 2R_E h_{oe}}$$

$$\therefore A_c = \frac{V_o}{V_s} = \frac{-I_L R_c}{V_s}$$

$$= \frac{-(h_{fe} - 2R_E h_{oe}) R_c}{2R_E(1+h_{fe}) + (R_s + h_{ie})(1+2R_E h_{oe})}$$

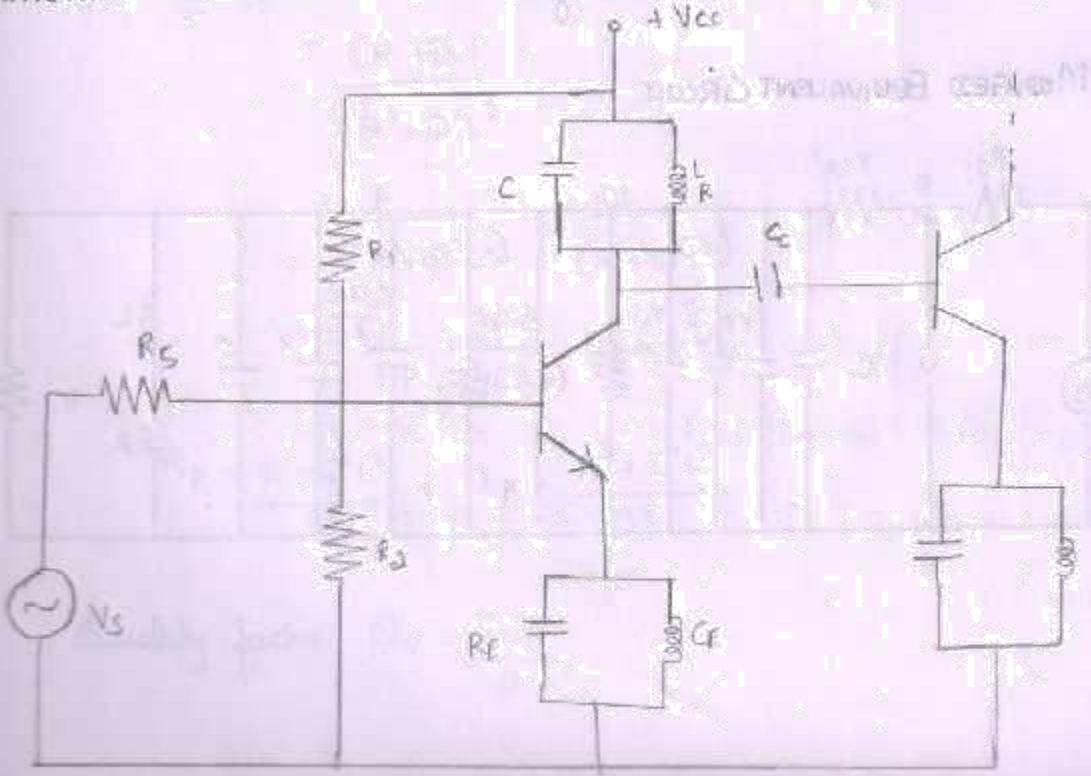
$$= \frac{R_c(2R_E h_{oe} - h_{fe})}{2R_E(1+h_{fe}) + (R_s+h_{ie})(1+2R_E h_{oe})}$$

$$A_c = \frac{-R_c h_{fe}}{R_s + h_{ie} + 2R_E(1+h_{fe})}$$

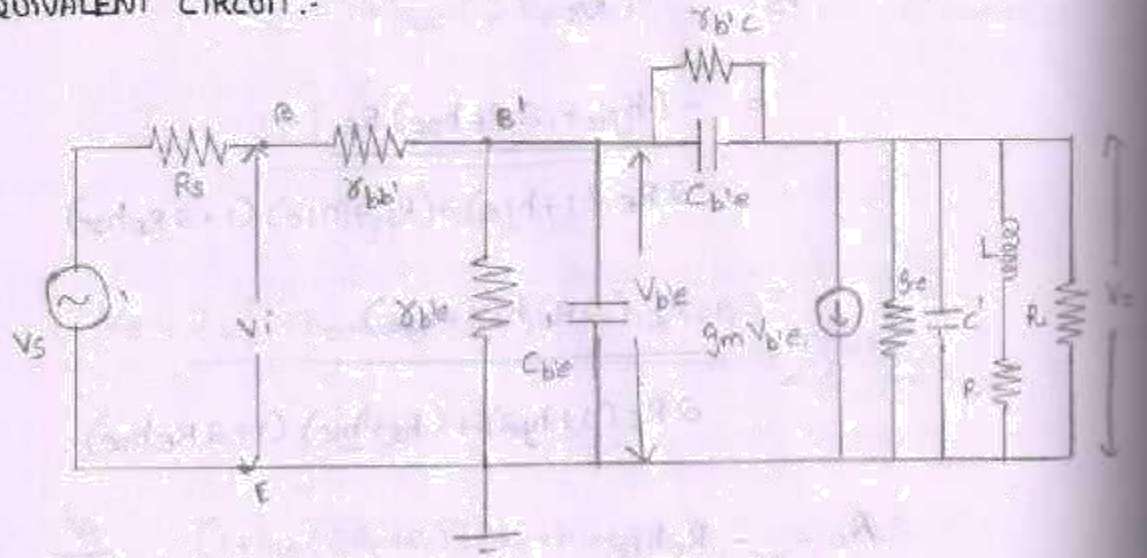
## SINGLE TUNED AMPLIFIERS:

⇒ Single tuned amplifiers use one parallel resonant circuits as the load impedance in each stage and all the tuned circuits are tuned to the same frequency.

## CAPACITIVE COUPLED SINGLE TUNED AMPLIFIER



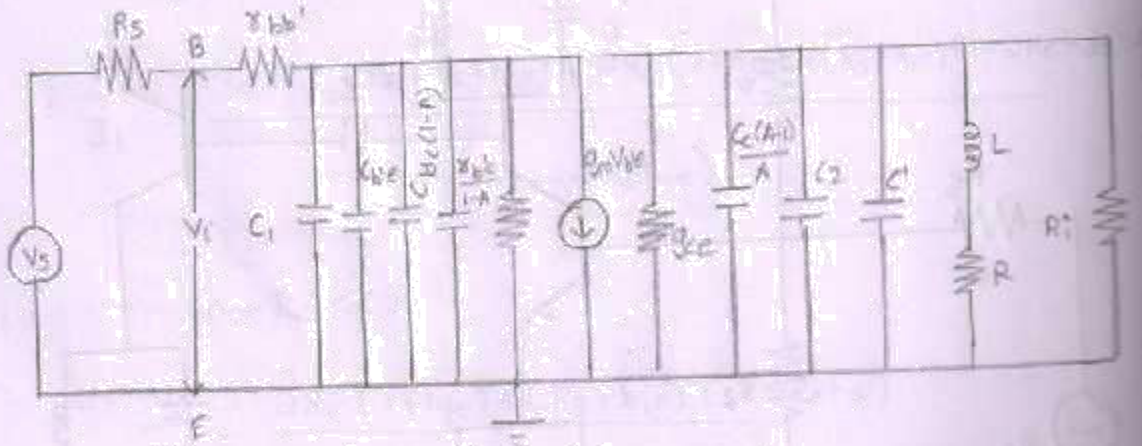
EQUIVALENT CIRCUIT :-




⇒ In the Capacitance coupled single tuned amplifier, output across the tuned circuit is coupled to the next stage through the coupling capacitor C. The tuned circuit formed by L and C' resonates at the frequency of operation.

→ In the equivalent circuit, $R_i$ is the input resistance of the next stage.

MODIFIED EQUIVALENT CIRCUIT



→ In the simplified Circuit, all the Capacitances in the input Circuit can be grouped together to form $C_S$ given by,

$$C_S = C_{b'e} + C_1 + C_{b'c}(1-A)$$

→ Similarly, all the Capacitances in the output Circuit can be grouped together to form C given by

$$C = C_{b'c}\left(\frac{A-1}{A}\right) + C_2 + C'$$

$$g_{ce} = \frac{1}{r_{ce}} = h_{oe} - g_m h_{re} \approx h_{oe} = \frac{1}{R_o}$$

→ The reactances of the bypass Capacitor $C_E$ and the Coupling Capacitor $C_c$ are negligibly small at the operating frequency and those elements can be neglected.

$$Y_i = \frac{1}{R+j\omega L} = \frac{(R-j\omega L)}{(R+j\omega L)(R-j\omega L)}$$

$$= \frac{(R-j\omega L)}{R^2+\omega^2 L^2}$$

$$= \frac{R}{(R^2+\omega^2L^2)} - j\frac{\omega L}{(R^2+\omega^2L^2)}$$

$$= \frac{1}{R_P} + \frac{1}{j\omega L_P}$$

$$R_P = \frac{R^2+\omega^2L^2}{R} \quad \& \quad L_P = \frac{R^2+\omega^2L^2}{\omega^2 L}$$

Quality factor, $Q_0 = \frac{\omega_0 L}{R}$

$$R_p = \frac{R^2 + \omega^2 L^2}{R}$$

$$= \frac{R\left(R + \frac{\omega^2 L^2}{R}\right)}{R}$$

$$R_p \simeq \frac{\omega^2 L^2}{R}$$

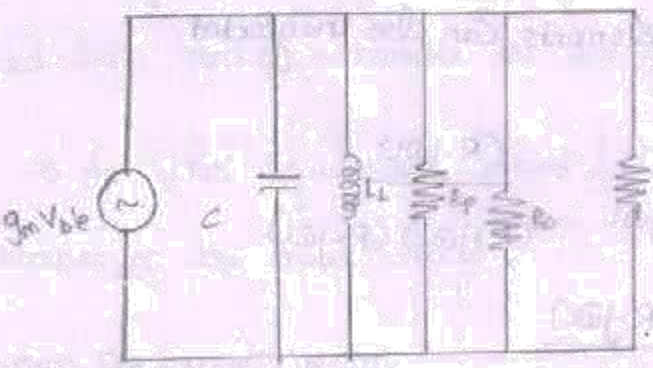
$$L_p = \frac{R^2 \omega^2 L^2}{\omega^2 L}$$

$\div$ num & den by $\omega^2 L$

$$L_p = \frac{R^2}{\omega^2 L} + L$$

$$\frac{1}{1}$$

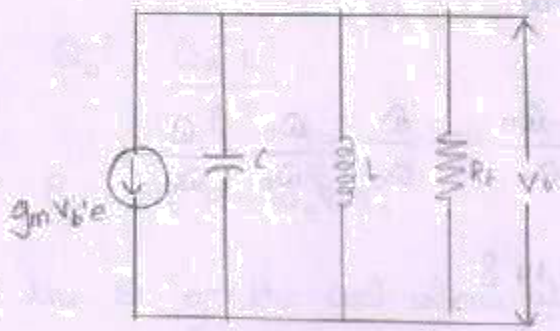
$$L_p = L$$




$$\frac{1}{R_t} = \frac{1}{R_o} + \frac{1}{R_p} + \frac{1}{R_i}$$

→ the effective quality factor or the Q-circuit magnification Q-circuit factor of the entire output circuit including $R_p$ and $R_i$ at resonant frequency $\omega_0$ is given by.

$Q_e$ = Susceptance of L (or) C / Conductance of $R_L$




$$Q_e = \omega_0 C R_L = \frac{R_L}{\omega_0 L}$$

From the output Circuit $V_0 = -g_m V_{b'e} Z$.

$$Y = \frac{1}{Z}$$

$$= \frac{1}{R_L} + \frac{1}{j\omega L} + j\omega C$$

$$= \frac{1}{R_L}\left[1 + \frac{R_L}{j\omega L} + j\omega C R_L\right]$$

Multiplying numerator and denominator by $\omega_0$.

$$Y = \frac{1}{R_L}\left[1 + \frac{R_L \omega_0}{j\omega L \omega_0} + \frac{j\omega\omega_0 C R_L}{\omega_0}\right]$$

$$\frac{R_L}{\omega_0 L} = \omega_0 C R_L = Q_e$$

$$Y = \frac{1 + jQ_e\left[\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right]}{R_L}$$

$$Z = \frac{1}{Y} = \frac{R_L}{1 + jQ_e\left[\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right]}$$

$\delta$ indicate the fractional frequency variation i.e., Variation in frequency is expressed as a fraction of the resonant frequency

$$\delta = \frac{\omega - \omega_0}{\omega_0} = \frac{\omega}{\omega_0} - \frac{\omega_0}{\omega_0} = \frac{\omega}{\omega_0} - 1$$

$$\frac{\omega}{\omega_0} = 1 + \delta$$

$$Z = \frac{R_L}{1 + jQ_e\left[(1+\delta) - \frac{1}{1+\delta}\right]}$$

$$= \frac{R_L}{1 + jQ_e\left[\frac{(1+\delta)^2 + 2\delta - 1)}{1+\delta}\right]}$$

$$Z = \frac{R_L}{1 + 2jQ_e\delta\left[\frac{\delta/2 + 1}{(1+\delta)}\right]}$$

$\boxed{\delta << 1}$

$$Z = \frac{R_L}{1 + j2Q_e\delta}$$

At resonance, $\omega = \omega_0$ & $\delta = 0$.

$$Z = R_L = R_0 \| R_p \| R$$

$$R_p = \frac{\omega_0^2 L^2}{R} = \frac{\omega_0 L}{\omega_0 CR}$$

$$= \frac{L}{CR}$$

$$R_p = \frac{\omega_0^2 L^2}{R}$$

$$Q_0 = \frac{\omega_0 L}{R}$$

$$Q_0^2 = \frac{\omega_0^2 L^2}{R^2}$$

$$R_p = Q_0^2 R = \omega_0 L Q_0$$

$Q_0$ is the Q of the coil alone at resonance

$$V_{b'e} = V_i \frac{r_{b'e}}{r_{bb'} + r_{b'e}}$$

$$V_0 = -g_m V_{b'e} Z$$

$$= -g_m \left( V_i \frac{r_{b'e}}{r_{bb'} + r_{b'e}} \right) Z$$

$$A = \frac{V_0}{V_i} = -g_m \left( \frac{r_{b'e}}{r_{bb'} + r_{b'e}} \right) Z$$

$$A = -g_m \left( \frac{r_{b'e}}{r_{bb'} + r_{b'e}} \right) \frac{R_L}{1 + j 2 Q_e \delta}$$

→ The Voltage gain at resonance $\delta = 0$ is given by,

$$A_{res} = -g_m \left( \frac{r_{be}}{r_{bb'} + r_{b'e}} \right) \cdot R_L$$

$$\frac{A}{A_{res}} = \frac{1}{1 + j 2 \delta Q_e}$$

$$\left|\frac{A}{A_{res}}\right| = \frac{1}{\sqrt{1+(2\delta Q_e)^2}}$$

$$\phi = -\tan^{-1} 2\delta Q_e$$

$\phi \rightarrow$ phase angle of $\frac{A}{A_{res}}$

At $\omega_1$, $\delta = \frac{1}{2Q_e}$

$$\left|\frac{A}{A_{res}}\right| = \frac{1}{\sqrt{2}} = 0.707$$

At $\omega_2$ above $\omega_0$,

$$\delta = \frac{1}{2Q_e}$$

$$\therefore \left|\frac{A}{A_{res}}\right| = \frac{1}{\sqrt{2}} = 0.707$$

The 3 dB bandwidth $\Delta\omega = \omega_2 - \omega_1$

$$= \frac{\left[(\omega_2 - \omega_0) + (\omega_0 - \omega_1)\right]\omega_0}{\omega_0}$$

$$= \left[\frac{(\omega_2 - \omega_0)}{\omega_0} + \frac{(\omega_0 - \omega_1)}{\omega_0}\right]\omega_0$$

$$\Delta\omega = [\delta + \delta]\omega_0$$

$$\Delta\omega = 2\delta\omega_0$$

But $\delta = \frac{1}{2Q_e}$

$$2\delta = \frac{1}{Q_e}$$

$$\Delta\omega = \frac{\omega_0}{Q_e}$$

$$Q_e = \omega_0 C R_L = \frac{R_L}{\omega_0 L}$$

$$\Delta\omega = \frac{\omega_0}{R_L \omega_0 C} = \frac{1}{R_L C} \text{ rad/s}$$

## GAIN AND FREQUENCY RESPONSE :

→ In order to obtain a high gain, several identical stages (or) tuned amplifiers can be used in cascade.

→ The overall voltage gain is the product of the voltage gain of individual stages.

→ The high voltage gain is accompanied by a narrow bandwidth.

→ the relative gain of the single tuned amplifier with respect to the gain at resonant frequency $f_0$.

$$\left| \frac{A}{A_{res}} \right| = \frac{1}{\sqrt{1+(2\delta Q_e)^2}}$$

→ The gain of the n stage cascaded amplifier becomes

$$\left| \frac{A}{A_{res}} \right|^n = \left[ \frac{1}{\sqrt{1+(2\delta Q_e)^2}} \right]^n$$

$$= \frac{1}{\left[1+(2\delta Q_e)^2\right]^{n/2}}$$

→ The 3 db frequencies for the n stage Cascaded amplifier can be found by equating $\left|\frac{A}{A_{mes}}\right|^n$ to $\frac{1}{\sqrt{2}}$

$$\left|\frac{A}{A_{mes}}\right|^n = \frac{1}{\left[\sqrt{1+(2\delta Q_e)^2}\right]^n} = \frac{1}{\sqrt{2}}$$

$$\left[\sqrt{1+(2\delta Q_e)^2}\right]^n = \sqrt{2}$$

$$1+(2\delta Q_e)^2 = 2^{1/n}$$

$$2\delta Q_e = \pm\sqrt{2^{1/n}-1}$$

→ Substituting for $\delta$, the fractional frequency Variation,

$$\delta = \frac{\omega-\omega_0}{\omega_0} ; \frac{f-f_0}{f_0}$$

$$2\left(\frac{f-f_0}{f_0}\right) Q_e = \pm\sqrt{2^{1/n}-1}$$

$$2(f-f_0) Q_e = \pm f_0 \sqrt{2^{1/n}-1}$$

$$f_2 - f_0 = \frac{f_0}{2Q_e}\sqrt{2^{1/n}-1}$$

→ The bandwidth of n stage identical amplifier is

$$B_{1n} = f_2 - f_1$$

$$= (f_2 - f_0) + (f_0 - f_1)$$

$$= \frac{f_0}{2Q_e}\sqrt{2^{1/n}-1} + \frac{f_0}{2Q_e}\sqrt{2^{1/n}-1}$$

$$= \frac{f_0}{2Q_e}\sqrt{2^{1/n}-1}$$

$$= B_1\sqrt{2^{1/n}-1}$$

→ where $B_{1n}$ is the bandwidth of n stages of the Cascade amplifier and $B_1$ is the bandwidth for single stage

→ Bandwidth of n stages $B_{1n}$ is equal to $B_1$ multiplied by a factor of $\sqrt{2^{1/n}-1}$

→ when $n = 2$; $\sqrt{2^{1/n}-1} = 0.643$

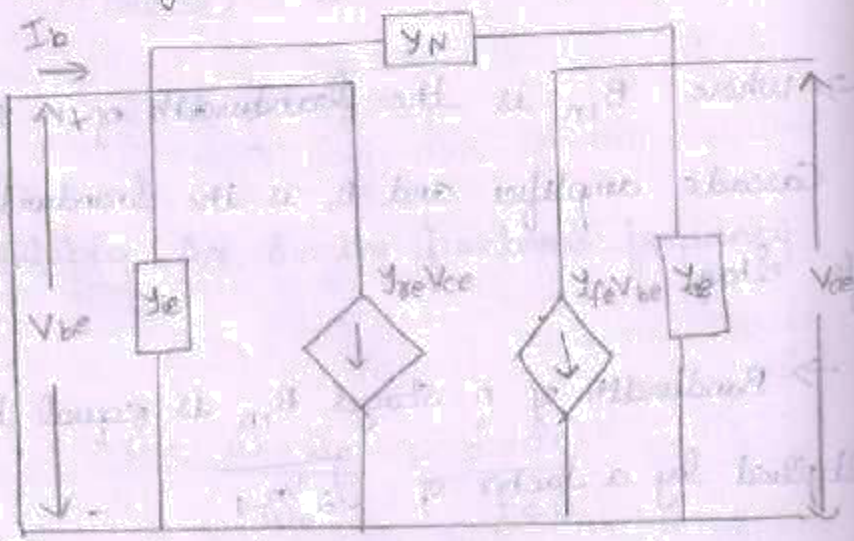
$n = 3$; $\sqrt{2^{1/n}-1} = 0.510$.

→ The bandwidth is reduced to 64.3% for two stages and 51% for three stages of Cascade amplifier.

## NEUTRALISATION :

→ The technique used for the elimination of potential Oscillation is called Neutralisation.

⇒ BJT and FET are potentially unstable over some frequency range due to the feedback parameters present in them. If the feedback can be cancelled by an additional feedback signal that is equal in magnitude and opposite in sign, the transistor becomes unilateral from input to output till the Oscillations completely stop. This is achieved by neutralisation.




$$Y_{re} = \left.\frac{I_b}{V_{ce}}\right|_{V_{be}=0}$$

→ with input terminal shorted.

$$I_b = y_{re} V_{ce} - Y_N V_{ce}$$

$$\therefore I_b = V_{ce}[Y_{re} - Y_N]$$

$$\frac{I_b}{V_{ce}} = Y_{re} - Y_N$$

$$Y'_{re} = Y_{re} - Y_N$$

⇒ for perfect neutralisation, $Y'_{re} = 0$ $\therefore Y_{re} = Y_N$. This indicates that Oscillation does not exist if the designed Circuit element matches $Y_{re}$ for all values of frequency and operating conditions

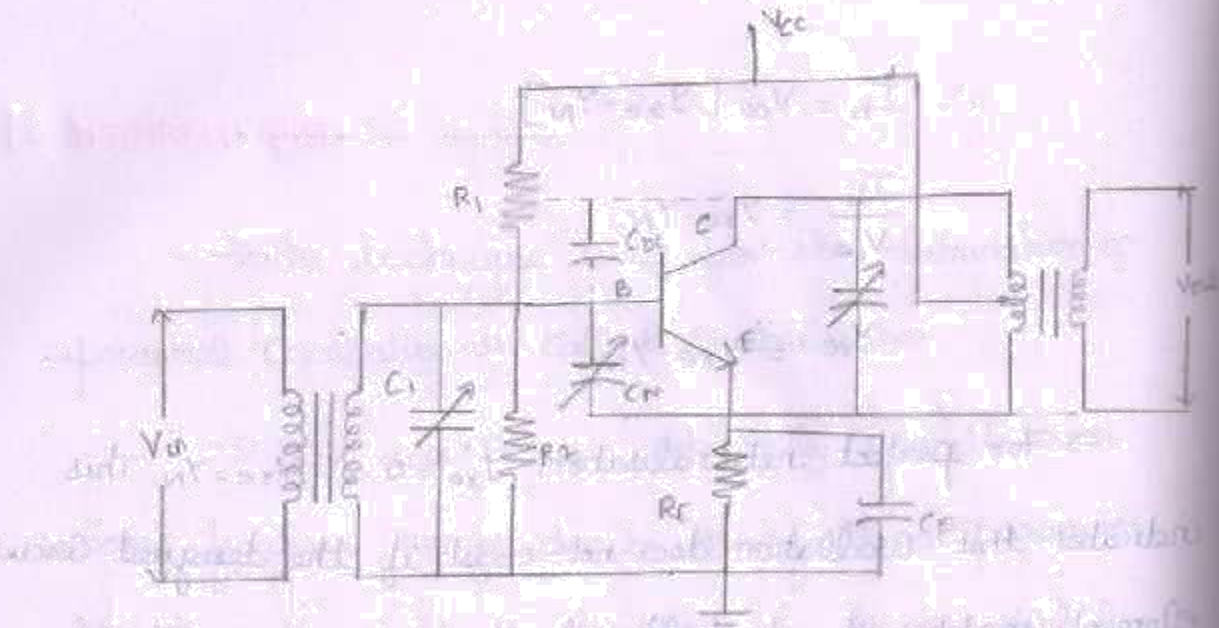
$$Y_{re} = -j\omega C_{re}$$

⇒ The fabrication of Capacitor is Complex, an inductor with negative Susceptance, $B = -j(1/\omega L)$ is preferred.

⇒ The inductor acts as a short Circuit at d.c Condition and need not be Considered. This Can be eliminated by using a fixed Capacitance that is transformer Coupled to for 180° phase shift to produce neutralisation over a limited frequency range.

Hazeltine Neutralisation method :-

⇒ This method is employed in tuned RF amplifiers to maintain stability.



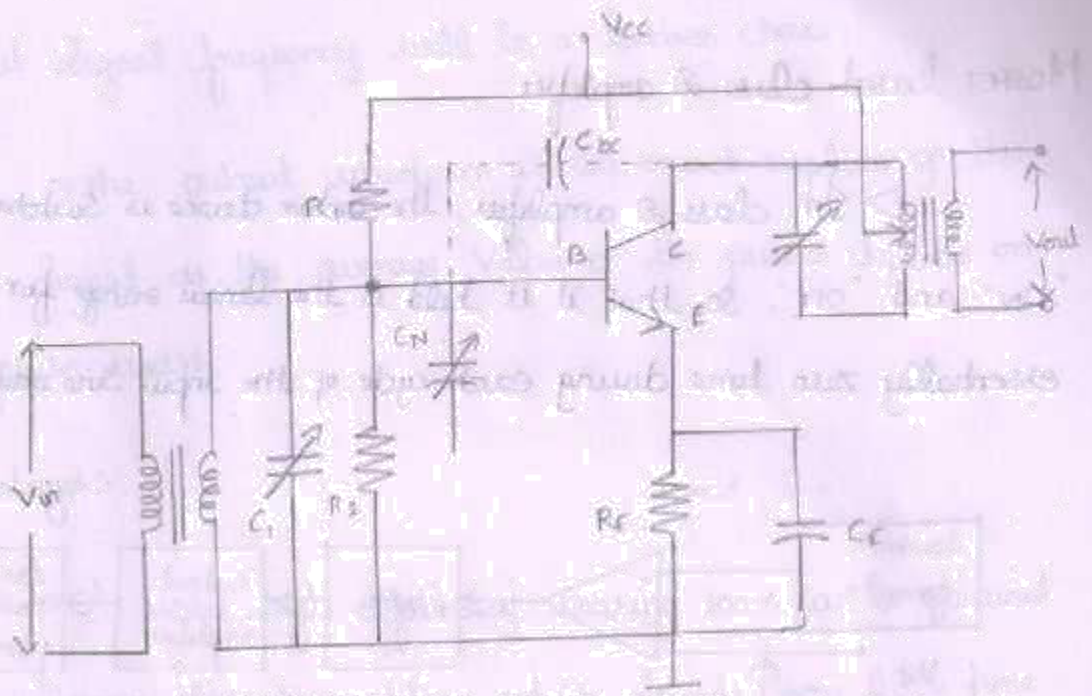

→ The undesired effect of the Collector to base Capacitance of the transistor is neutralised by introducing a signal which cancels the signal coupled through the Collector to base Capacitance.

→ $C_N$ is connected from the bottom of coil to the base of the transistor. The neutralisation process is achieved by $C_N$. It introduces a signal to the base of the transistor such that is cancels out the signal fed to the base by $C_{bc}$.

→ A Vaccable Capacitor is used for Neutralisation as the Value of $C_{bc}$ changes with time. By adjusting $C_N$, exact neutralisation is achieved.

Neutrodyne neutralisation Technique

→ The modified Version of Hazeltine technique is the Neutrodyne neutralisation technique.




→ $C_N$ is connected to the lower end of the secondary coil of the next stage. It is insensitive to any variation in the supply voltage $V_{cc}$ and provides higher stabilisation for the tuned amplifier.

## Power Amplifier

→ It is designed to switch large currents ON & OFF using MOSFET devices

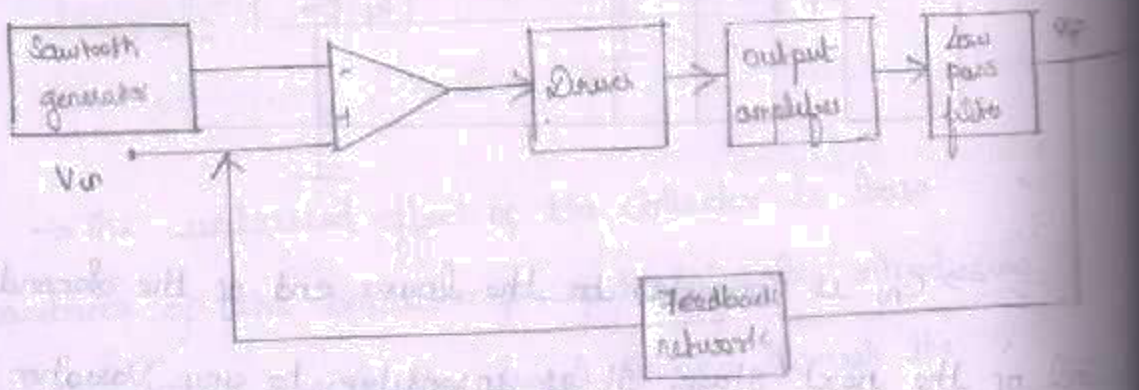
→ MOSFET based class-D amplifier is commonly employed.

→ The advantage of using MOSFET is that the turn-off time is not delayed by minority carrier storage as it is in BJT.

→ Current in MOSFET is due to majority carriers only and they are not subjected to thermal runaway

Mosfet based class-D amplifier

→ In class-D amplifier, the active device is switched "ON" and "OFF". So that it is held in the linear range for essentially zero time during each cycle of the input sine wave




→ The analog signal modulates the saw tooth waveform so that a pulse width modulated output is obtained, which drives the class D output amplifier, causing it to switch ON and OFF as the pulses switch between high & low

→ A class D amplifier must have a filter circuit to extract the signal to be amplified from the pulsed waveform.

→ As the signal may have many frequency components a low pass filter having a cut off frequency nearer to the

highest signal frequency will be a better choice.

⇒ The output waveform is an exact replica of the input signal as the average value of the pulses depends on the pulse width.

**Advantages:-**

⇒ A very high efficiency nearing 100% can be obtained by employing class D amplifiers which spends very little time in active region, which minimises the power dissipation

**Drawbacks:-**

⇒ Filters with sharp cutoff frequencies are complex in design. High speed switching of large current generates noise through electromagnetic coupling called electromagnetic interference

Unit-IV
Completed

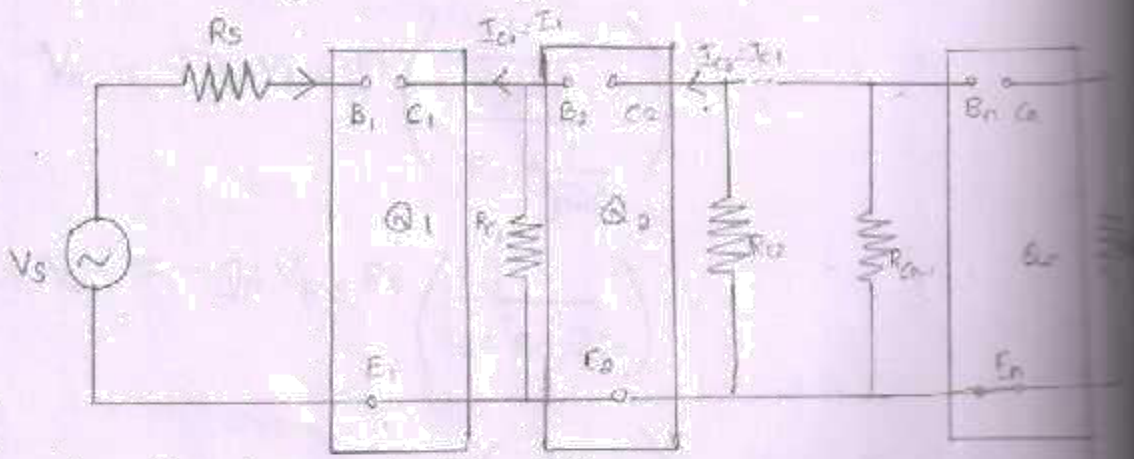
UNIT - 4 -

MULTISTAGE AMPLIFIERS & DIFFERENTIAL AMPLIFIER

BIMOS CASCADE AMPLIFIER:

→ When the amplification of a single stage amplifier is not sufficient for a particular purpose (or) when the input (or) output impedance is not of correct magnitude for the intended application, two (or) more stages may be connected in cascade.

→ The main function of cascading stages is that the larger overall gain is achieved




Voltage gain:-

→ The resultant voltage gain is given by the product of the individual voltage gains of each stage

# UNIT - 5. FEEDBACK AMPLIFIERS & OSCILLATORS

## Advantage of Negative feedback :

- ⇒ Better stabilized Voltage gain
- ⇒ Enhanced frequency response
- ⇒ Higher input impedance
- ⇒ Lower output impedance
- ⇒ Reduction in noise
- ⇒ Increase in linearity

## Voltage - Series Feedback :

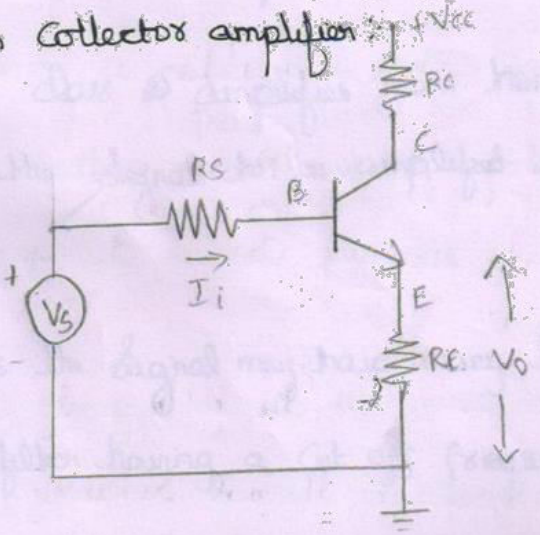
⇒ The examples of Voltage - Series topology are

i) BJT Common - Collector amplifier

ii) FET Common - drain amplifier

iii) Voltage - Series feedback pair

i) BJT - Common Collector amplifier :



→ The voltage gain with feedback is given by,

$$A_{vf} = \frac{A_v}{D} = \frac{h_{fe} R_E}{R_S + h_{ie} + h_{fe} R_E}$$

→ If $h_{fe} R_E \gg R_S + h_{ie}$, then $A_{vf} \approx 1$.

→ The input resistance without feedback is given by,

$A_{vf} = 1$ $R_i = R_S + h_{ie}$

→ The input resistance with feedback is given by,

$$R_{if} = R_i D = (R_S + h_{ie}) \times \frac{R_S + h_{ie} + h_{fe} R_E}{R_S + h_{ie}}$$

$$= R_S + h_{ie} + h_{fe} R_E$$

→ The output resistance with feedback is given by,

$$R_{of} = \frac{R_o}{1 + \beta A_v} = \frac{\infty}{\infty}$$

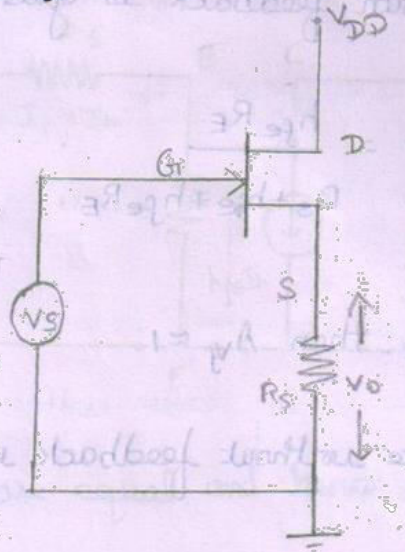
→ By considering the external load,

$$R'_{of} = \frac{R'_o}{D} = \frac{R_E (R_S + h_{ie})}{R_S + h_{ie} + h_{fe} R_E}$$

where $R_o' = R_L = R_E$

$$R_{of} = \lim_{R_L \to \infty} R'_{of} = \frac{R_S + h_{ie}}{h_{fe}}$$

ii) FET Source follower:




⇒ The feedback signal is the voltage $V_f$ across $R_s$ and the sampled signal is the output voltage $V_o$ across $R_s$.

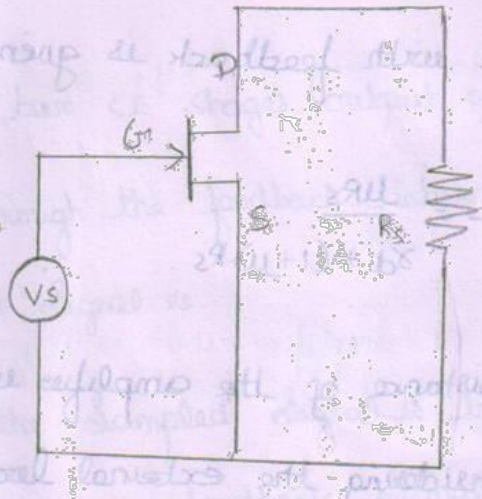
⇒ The basic amplifier without feedback is obtained by

To find the input circuit:

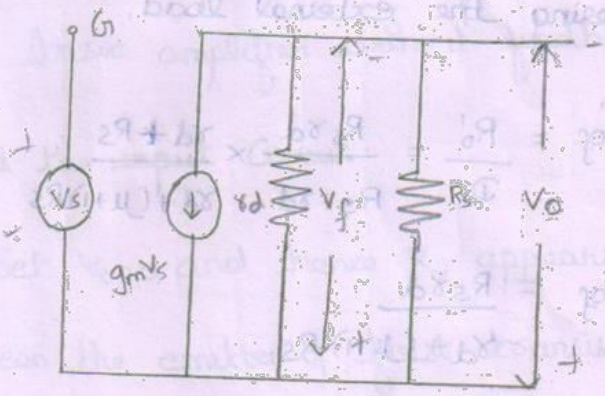
⇒ Set $V_o = 0$ and hence $V_s$ appears directly b/w G and S at the input side

To find the output circuit:

⇒ Set $I_i = 0$ and hence $R_s$ appears only in the output loop




→ The equivalent circuit after replacing the FET by its low frequency model is given by.




→ Here $V_f$ and $V_o$ are equal and hence $\beta = V_f/V_o = 1$

→ The voltage gain without feedback is given by.

$$A_V = \frac{V_o}{V_i} = \frac{g_m V_{gs} r_d R_s}{(r_d + R_s)V_s} = \frac{\mu R_s}{r_d + R_s}$$

→ where $\mu = g_m \times r_d$ and $V_s = V_{gs}$.

→ The desensitivity is given by,

$$D = 1 + \beta A_V = 1 + \frac{\mu R_s}{r_d + R_s} = \frac{r_d + (1+\mu) R_s}{r_d + R_s}$$

$\beta = 1$

→ The voltage gain with feedback is given by,

$$A_{Vf} = \frac{A_V}{D} = \frac{\mu R_s}{r_d + (1+\mu) R_s}$$

⇒ The output resistance of the amplifier with feedback without considering the external load resistance

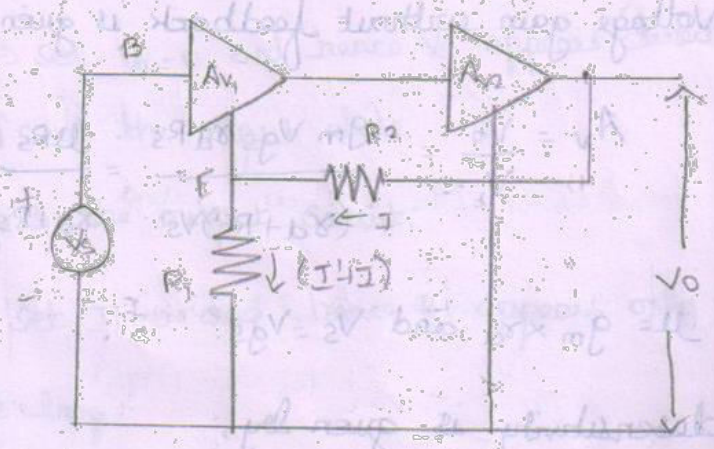
$$R_{of} = \frac{R_o}{1+\beta A_V} = \frac{r_d}{1+\mu}$$

⇒ By considering the external load

$$R'_{of} = \frac{R'_o}{D} = \frac{R_s r_d}{R_s + r_d} \times \frac{r_d + R_s}{r_d + (\mu+1) R_s}$$

$$R_{of} = \frac{R_s r_d}{r_d + (\mu+1) R_s}$$

ii) Voltage series feedback pair :-



→ In two CE stages output of the second stage is returned through the feedback network $R_1 - R_2$ in opposition to the input signal $V_s$.

→ As the sampled signal is taken directly from the output node and the feedback signal is applied in series with the external excitation, this is another case of voltage series feedback topology.

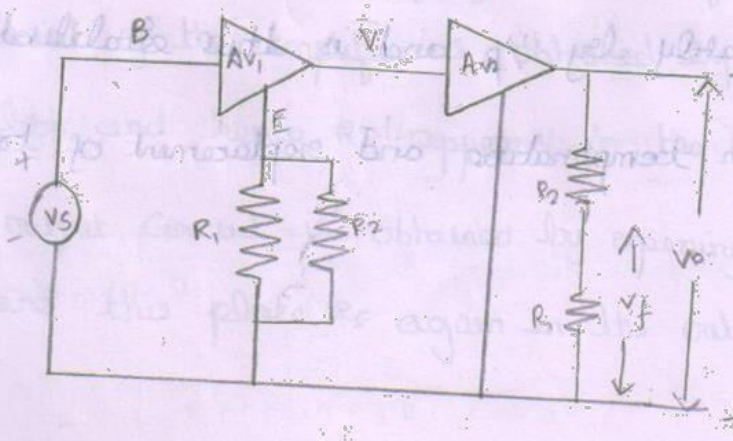
→ The basic amplifier without feedback is given by,

i) To find the input circuit.

Set $V_0 = 0$ and hence $R_2$ appears in parallel with $R_1$ between the emitter of first transistor and ground.

ii) To find the output circuit

Set $I_i = 0$ and hence $R_1$ is placed in series with $R_2$ between the collector of second transistor and ground.



→ In two CE stages output of the second stage is returned through the feedback network $R_1 - R_2$ in opposition to the input signal Vs.

→ As the sampled signal is taken directly from the output node and the feedback signal is applied in series with the external excitation, this is another case of voltage series feedback topology.

→ The basic amplifier without feedback is given by:

i) To find the input circuit.

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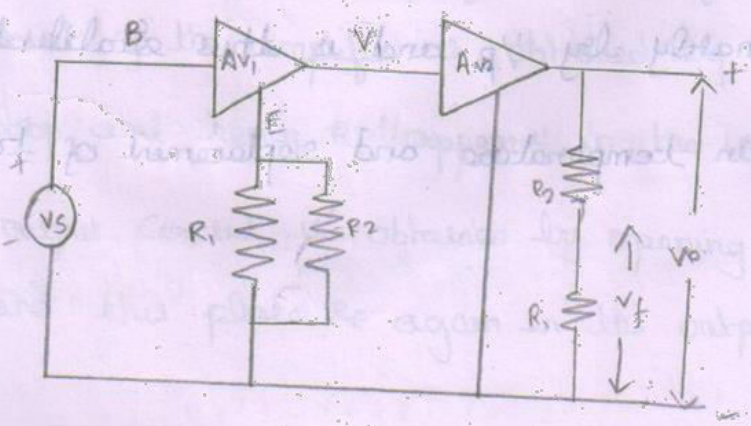
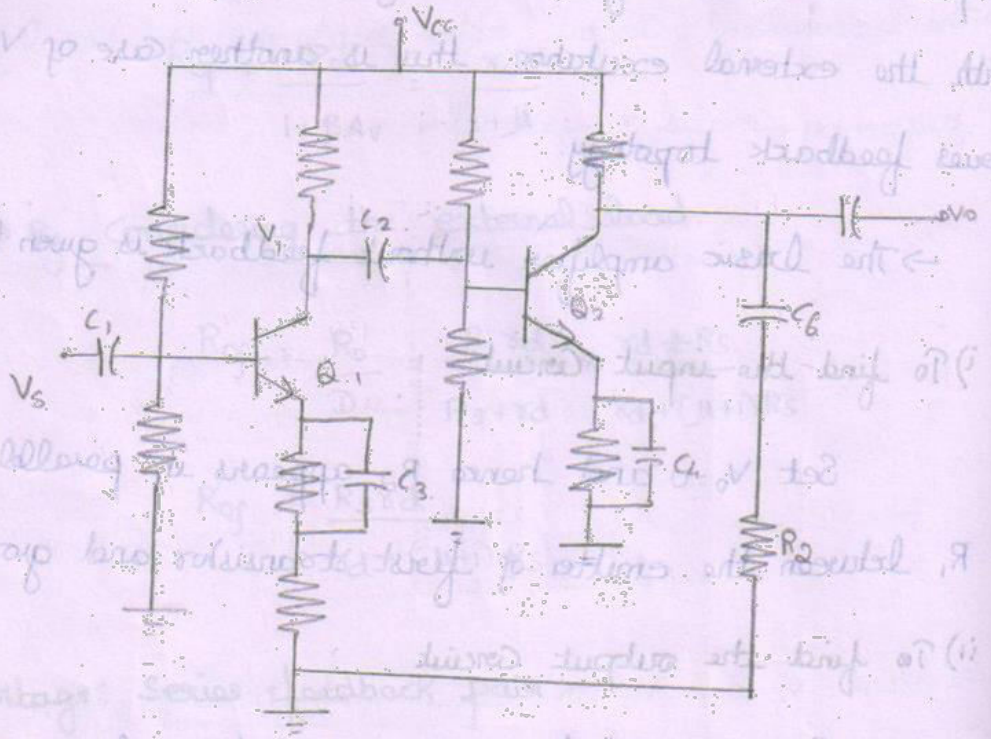
Set $I_i = 0$ and hence $R_2$ is placed in series with $R_2$ between the collector of second transistor and ground.



→ The feedback factor is given by,

$$\beta = \frac{V_f}{V_o} = \frac{R_1}{R_1 + R_2}$$

→ The two stage CE amplifier with voltage series feedback is given by,




→ For this amplifier the voltage gain $A_f$ is given approximately by $1/\beta$ and is thus stabilized against changes in temperature and replacement of transistor.

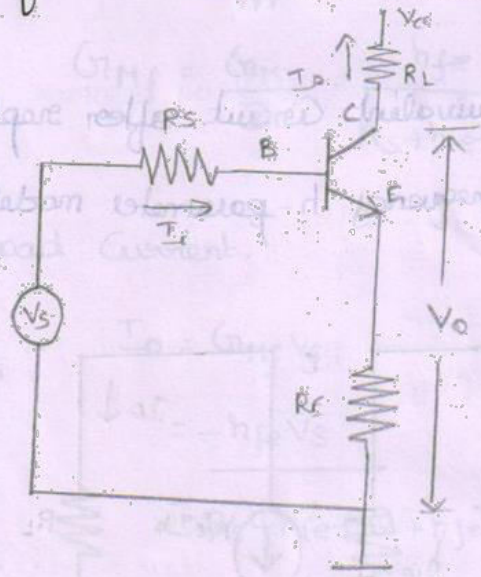
Current Series feedback:

→ The examples of this topology are

i) Common emitter amplifier

ii) FET Common source amplifier

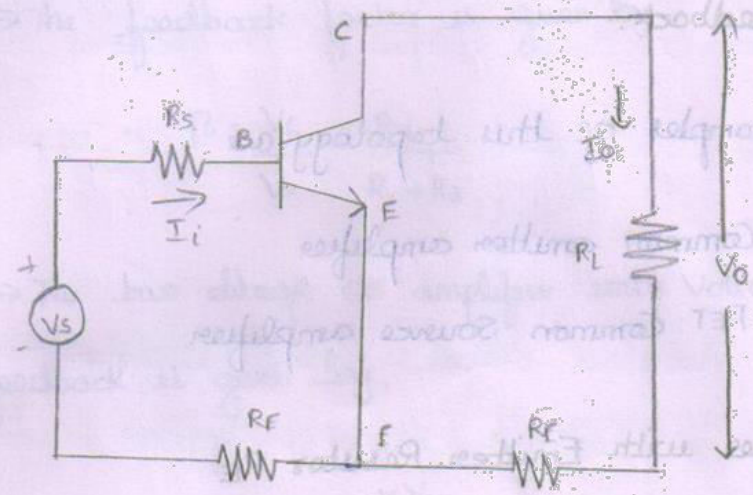
i) BJT CE amplifier with Emitter Resistor $R_E$



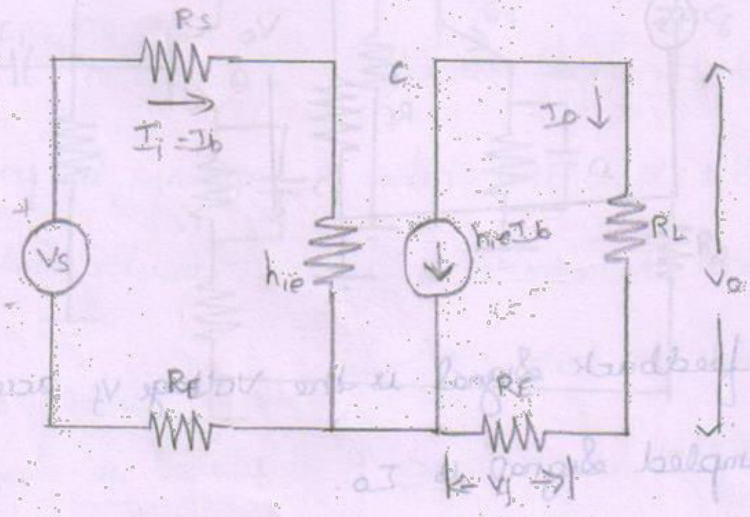

→ The feedback signal is the voltage $V_f$ across $R_E$ and the sampled signal is $I_o$.

→ To obtain the basic amplifier without feedback, the input circuit of the amplifier is obtained by opening the output loop and hence $R_E$ appears in the input side.

→ The output circuit is obtained by opening the input loop and this place $R_E$ again in the output side




→ The resultant equivalent circuit after replacing the transistor by its low frequency h-parameter model is given by.




$$\beta = \frac{V_f}{I_o} = \frac{-I_o R_F}{I_o} = -R_F$$

→ Transconductance without feedback is given by,

$$G_M = \frac{I_o}{V_i} = \frac{-h_{fe} I_b}{V_s} = \frac{-h_{fe}}{R_s + h_{ie} + R_F}$$

$$V_s = I_b (R_s + h_{ie} + R_F)$$

⇒ The desensitivity is given by,

$$D = 1 + \beta G_M$$

$$= 1 + \frac{h_{fe} R_E}{R_S + h_{ie} + R_E} = \frac{R_S + h_{ie} + (1+h_{fe}) R_E}{R_S + h_{ie} + R_E}$$

⇒ The transconductance with feedback is,

$$G_{Mf} = \frac{G_M}{D} = \frac{-h_{fe}}{R_S + h_{ie} + (1+h_{fe}) R_E}$$

⇒ The load Current,

$$I_o = G_{Mf} V_s$$

$$= \frac{-h_{fe} V_s}{R_S + h_{ie} + (1+h_{fe}) R_E}$$

$$\simeq \frac{-V_s}{R_E}$$

⇒ The Voltage gain is given by,

$$A_{Vf} = \frac{I_o R_L}{V_s} = G_{Mf} R_L$$

$$= \frac{-h_{fe} R_L}{R_S + h_{ie} + (1+h_{fe}) R_E}$$

⇒ The input resistance without feedback is given by,

$$R_i = R_S + h_{ie} + R_E$$

$\Rightarrow R_{if} = R_i \supset = R_S + h_{ie} + (1+h_{fe})R_E$

$\Rightarrow$ The output resistance of the amplifier with feedback without considering the external load resistance.

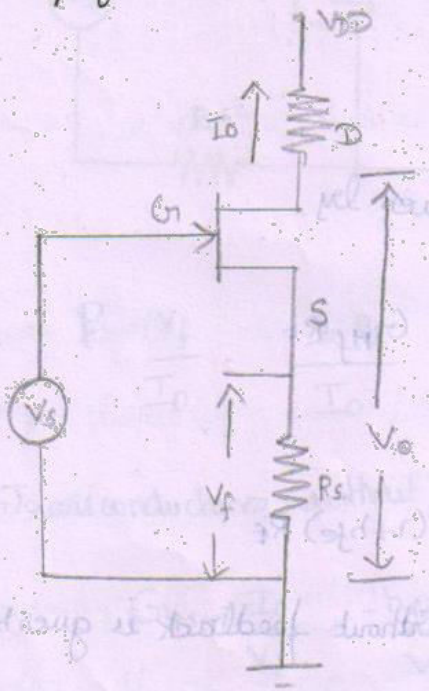
$$R_{of} = R_o(1+\beta G_m) \rightarrow \infty$$

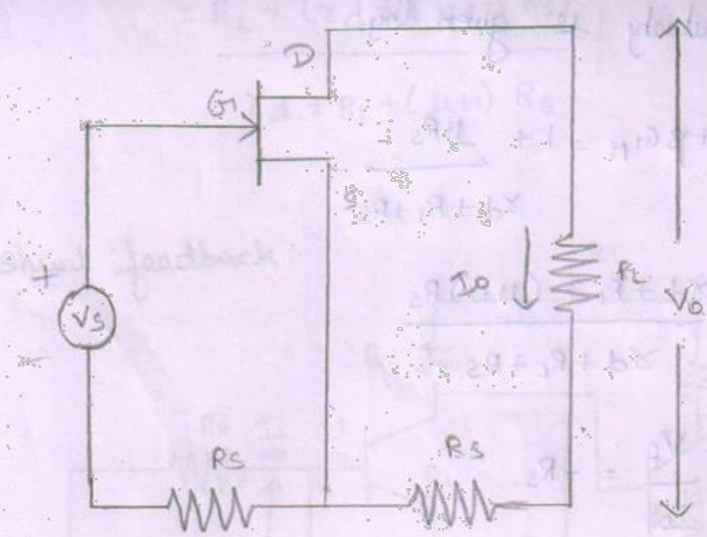
$\Rightarrow$ By Considering the external load resistance.

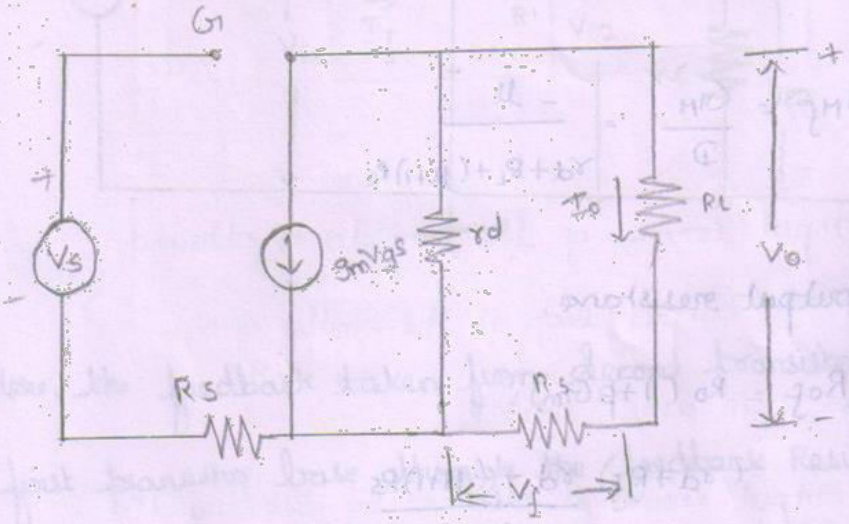
$$R'_{of} = R_L \parallel R_{of} = R_L$$

$$R'_{of} = R'_o \frac{1+\beta G_m}{1+\beta G_M}$$

(ii) FET CS Amplifier with Source Resistor $R_S$






→ without feedback, $V_i = V_s$ and the transconductance without feedback is given by

$$G_M = \frac{I_o}{V_i} = \frac{I_o}{V_s} = \frac{-g_m V_{gs} r_d}{r_d + R_L + R_s} \times \frac{1}{V_s}$$

$$= \frac{-\mu}{r_d + R_L + R_s}$$

where $\mu = g_m \times r_d$ and $V_s = V_{gs}$

→ The desensitivity is given by

$$D = 1 + \beta G_M = 1 + \frac{\mu R_S}{r_d + R_L + R_S}$$

$$= \frac{r_d + R_L + (\mu+1) R_S}{r_d + R_L + R_S}$$

where $\beta = \frac{V_f}{I_O} = -R_S$.

→ The transconductance with feedback is given by,

$$G_{Mf} = \frac{G_M}{D} = \frac{-\mu}{r_d + R_L + (\mu+1) R_S}$$

→ The output resistance,

$$R_{of} = R_o (1 + \beta G_m)$$

$$= (r_d + R_S) \frac{r_d + (\mu+1) R_S}{r_d + R_S}$$

$$= r_d + (\mu+1) R_S$$

→ $R'_{of} = R_{of} \parallel R_L$

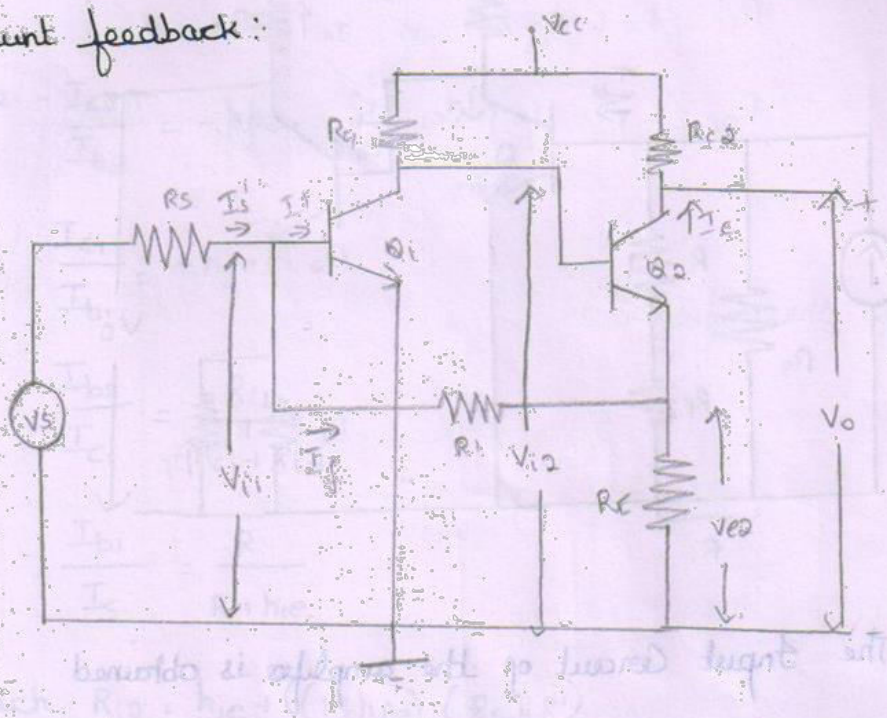
$$= \frac{R_L \times (r_d + \mu+1) R_S)}{R_L + r_d + (\mu+1) R_S}$$

$$R'_{of} = R_o \frac{1 + \beta G_m}{D}$$

$$= \frac{(r_d + R_S) R_L}{r_d + R_S + R_L} \times \frac{r_d + (\mu+1) R_S}{r_d + R_S} \times \frac{r_d + R_L + R_S}{r_d + R_L + (\mu+1) R_S}$$

$$= \frac{R_L + (r_d + (\mu+1) R_s)}{r_d + R_L + (\mu+1) R_s}$$

Current shunt feedback:



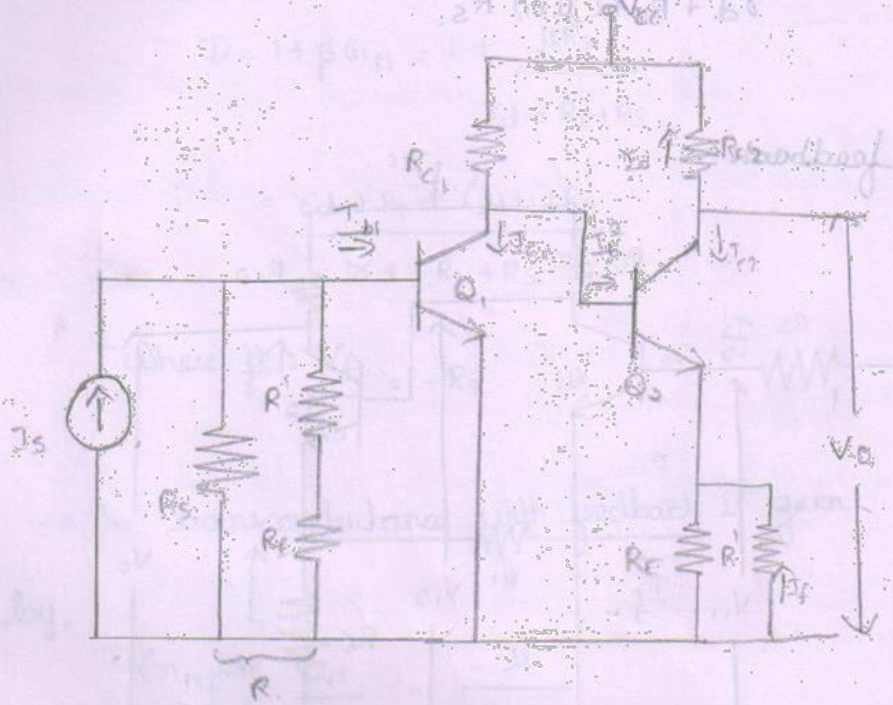

⇒ Here, the feedback taken from second transistor emitter to the first transistor base through the feedback Resistor R'.

→ The output voltage of $Q_2$ is much larger than $V_{i1}$ because of its high voltage gain and it is 180° out of phase with $V_{i1}$.

→ The voltage across emitter of $Q_2$ is only slightly smaller than $V_{i2}$ and these voltages are in phase.

→ It corresponds to current shunt topology. Since the sampled signal is taken from the output loop and the feedback signal is connected directly to the input node

Basic amplifier without feedback




→ The input circuit of the amplifier is obtained by opening the output loop at the emitter of $Q_2$ which places $R'$ in series with $R_E$.

→ The output circuit is obtained by shorting the input node which places $R'$ in parallel with $R_E$.

$$I_f = \frac{V_{in} - V_{e2}}{R'} \simeq \frac{V_{e2}}{R'} - \frac{(I_o - I_f)R_E}{R'}$$

$$\therefore I_f = \frac{R_E I_o}{R' + R_E} = \beta I_o$$

→ where $\beta = \frac{R_E}{R' + R_E}$

→ The transfer Current gain without feedback is given by,

$$A_I = \frac{-I_{c2}}{I_s} = \frac{-I_{c2}}{I_{b2}} \frac{I_{b2}}{I_{c1}} \frac{I_{c1}}{I_{b1}} \frac{I_{b1}}{I_s}$$

Where $\frac{-I_{c2}}{I_{b2}} = -h_{fe}$,

$$\frac{I_{c1}}{I_{b1}} = +h_{fe},$$

$$\frac{I_{b2}}{I_{c1}} = \frac{-R_{c1}}{R_{c1}+R_{i2}}$$

$$\frac{I_{b1}}{I_s} = \frac{R}{R+h_{ie}}$$

in which $R_{i2} = h_{ie} + (1+h_{fe})(R_E \parallel R')$

$$R = R_s \parallel (R' + R_E)$$

→ The desensitivity is given by,

$$D = 1 + \beta A_I$$

where $\beta = R_E / (R' + R_E)$

→ The Current gain with feedback is,

$$A_{vf} = \frac{V_o}{V_s} = \frac{-I_{c2} R_{c2}}{I_s R_s} = \frac{A_I R_{c2}}{R_s} = \frac{R_{c2}}{\beta R_s}$$

→ The input impedance without feedback,

$$R_i = R \parallel h_{ie}$$

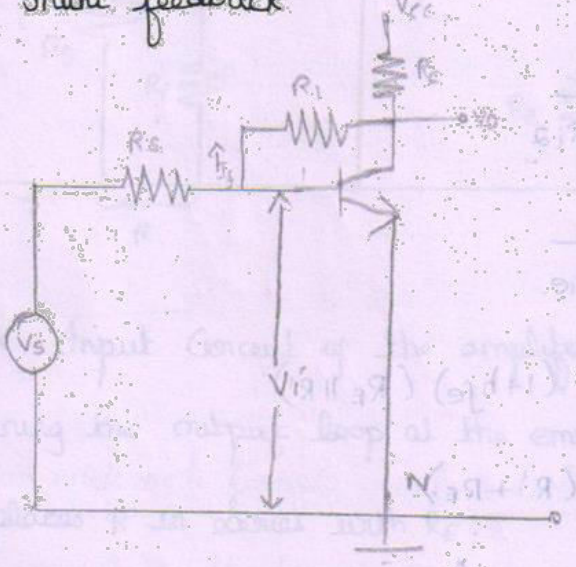
$$R_{if} = R_i / D$$

→ The output resistance by considering load resistance and without considering load resistance is given by,

$$R_{of} = R_o (1+\beta A_i) \to \infty$$

$$R'_{of} = R'_o \frac{1+\beta A_i}{1+\beta A_i} = R'_o = R_{12}$$

Voltage shunt feedback



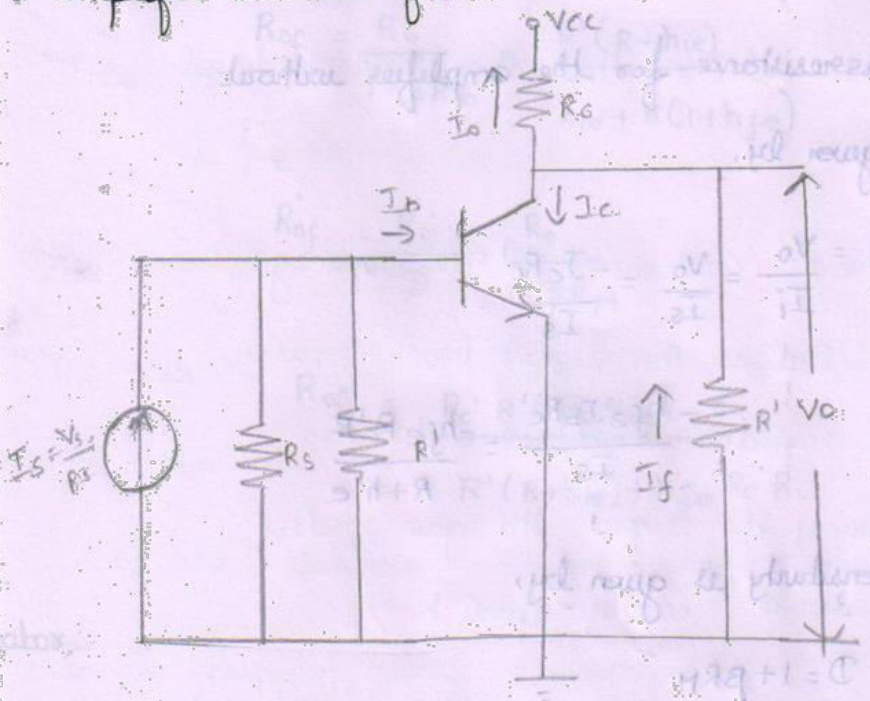

→ The sampled signal is taken directly from the output node and the feedback signal is connected directly to the input node.

→ $V_o$ is much greater than input voltage and is 180° out of phase with $V_i$. Hence,

$$I_f = \frac{V_i - V_o}{R'} \approx -\frac{V_o}{R'} = \beta V_o$$

where $\beta = \frac{I_f}{V_o} = -\frac{1}{R'}$

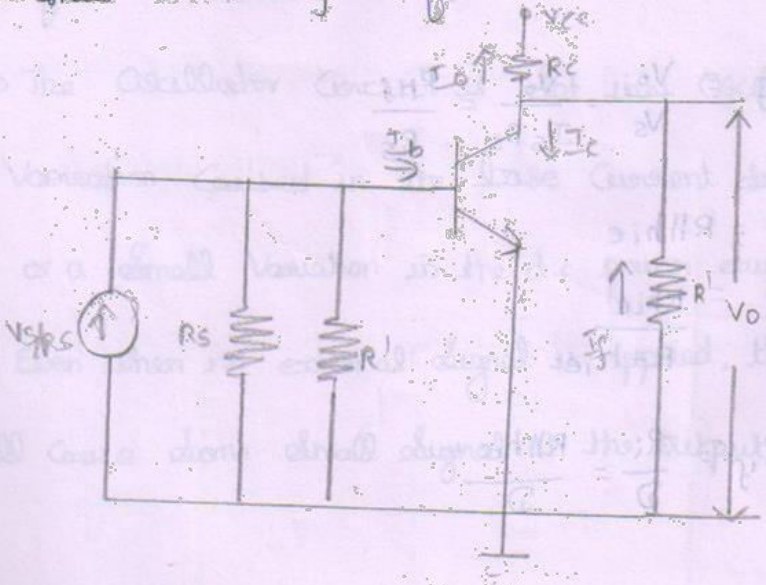
Basic amplifier without feedback :




⇒ The input Circuit is obtained by shorting the output node and thus R' Connected between base and emitter of the transistor.

⇒ The output Circuit is found by shorting the input node and thus Connecting R' from Collector to emitter

⇒



$$\beta = \frac{I_f}{V_o} = -\frac{1}{R'}$$

→ The transresistance for the amplifier without feedback is given by,

$$R_M = \frac{V_o}{I_i} = \frac{V_o}{I_s} = \frac{-I_c R_c'}{I_s}$$

$$= -\frac{h_{fe} I_b R_c'}{I_s} = \frac{-h_{fe} R_c' R}{R + h_{ie}}$$

→ The desensitivity is given by,

$$D = 1 + \beta R_M$$

$$= 1 + \frac{h_{fe} R_c' R}{R'(R + h_{ie})}$$

$$R_{Mf} = \frac{R_M}{D}$$

$$= \frac{-h_{fe} R_c' R R'}{R'(R + h_{ie}) + h_{fe} R_c' R}$$

$$A_{vf} = \frac{V_o}{V_s} = \frac{V_o}{I_s R_s} = \frac{R_{Mf}}{R_s}$$

$$R_i = R \| h_{ie}$$

$$= \frac{R h_{ie}}{R + h_{ie}}$$

$$R_{if} = \frac{R_i}{D} = \frac{R \| h_{ie}}{D}$$

→ The output resistance is given by,

$$R_{of} = \frac{R_o}{1+\beta R_m} = \frac{R'(R+h_{ie})}{h_{ie}+R(1+h_{fe})}$$

$$R'_{of} = \frac{R'_o}{D} = \frac{R'_o}{1+\beta R_m}$$

$$R'_{of} = \frac{R'_c R'(R+h_{ie})}{R'(R+h_{ie})+h_{fe} R'_c R}$$

Oscillator :-

→ The Circuit which is used to generate a periodic voltage without an a.c input signal is called an Oscillator. To generate the periodic voltage, the Circuit is supplied with energy from d.c Source.

Condition for Oscillation :-

→ The Oscillator Circuit is set into Oscillations by a random Variation Caused in the base Current due to noise Component or a Small Variation in the d.c power Supply.

→ Even when no external signal is applied, the ever present noise will cause some small signal at the output of the amplifier

→ when the amplifier is tuned at a particular frequency, the output signal is fedback to the input with proper phase relation, then this feedback signal becomes larger.

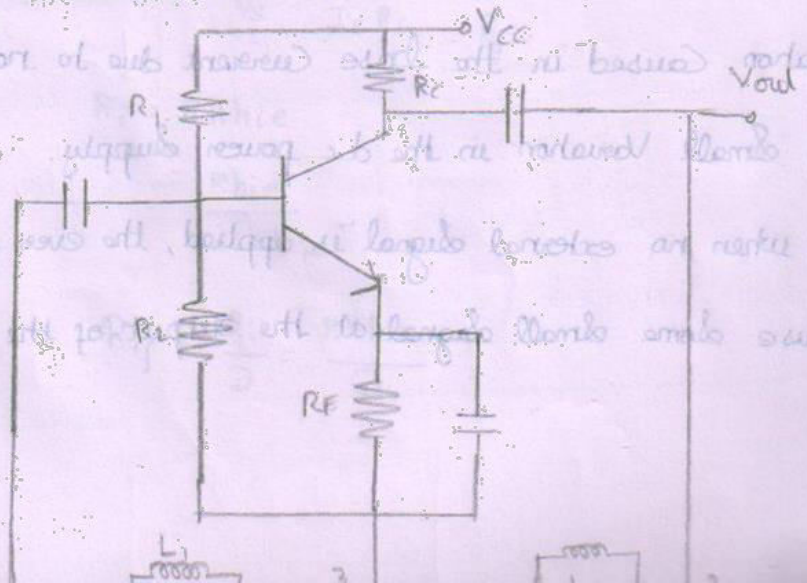
→ This process continues and the output goes on increasing. But as the signal level increases, the gain of the amplifier decreases and at a particular value of the output, the gain of the amplifier is reduced exactly equal to $1/\beta$.

→ The essential condition for maintaing Oscillation is.

i) $|A\beta| = 1$ i.e, the magnitude of the loop gain must be unity

ii) The total phase shift around the closed loop is zero or 360 degrees.

Hartley Oscillator:-



$Z_1, Z_2$ → Inductors

$Z_3$ → Capacitor

$C_E$ → Bypass Capacitor

$C_{c_1}, C_{c_2}$ → coupling Capacitor

→ The resistor $R_1, R_2, R_E$ provide the necessary d.c bias to the transistor.

→ $L_1, L_2$ and C determines the frequency of the Oscillator.

→ When the supply voltage is switched ON, a transient current is produced in the tank circuit and then damped harmonic oscillations are produced in the circuit.

→ The Oscillatory current produces a.c voltages across $L_1$ and $L_2$.

→ As 3 is earthed, it is at zero potential.

→ If 1 is positive with respect to 3 at any instant, 2 will be at negative potential with respect to 3 at the same instant.

→ Thus the phase difference between 1 and 2 is always 180°.

→ The frequency of Oscillation is $f_o = \frac{1}{2\pi\sqrt{LC}}$

where $L = L_1 + L_2 + 2M$

⇒ The condition for sustained Oscillation is

$$h_{fe} \geq \frac{L_1+M}{L_2+M}$$

Analysis :-

$$Z_1 = j\omega L_1 + j\omega M$$

$$Z_2 = j\omega L_2 + j\omega M$$

$$Z_3 = \frac{1}{j\omega C} = \frac{-j}{\omega C}$$

$$j\omega h_{ie}\left[L_1+L_2+2M-\frac{1}{\omega^2 C}\right]-\omega^2(L_1+M)$$

$$\left[(L_2+M)(1+h_{fe})-\frac{1}{\omega^2 C}\right]=0$$

⇒ The frequency of Oscillation $f_0 = \frac{\omega_0}{2\pi}$ is determined by equating the imaginary part of the equation to zero

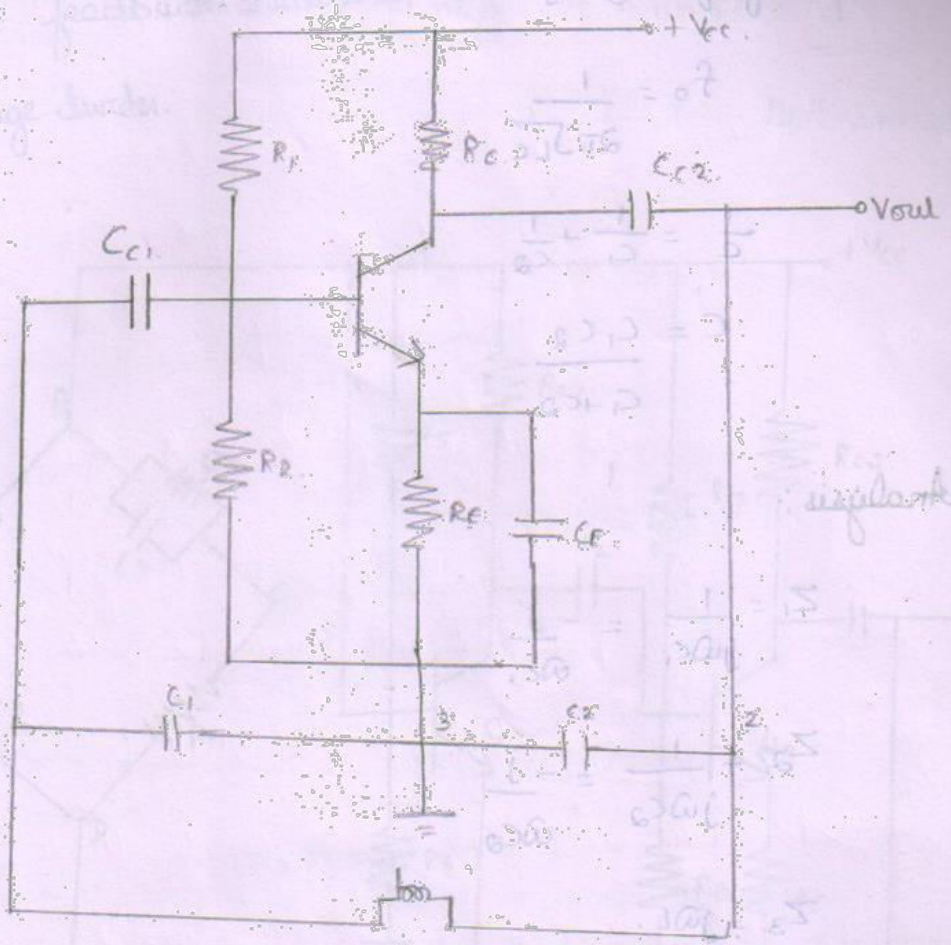
$$\left[L_1+L_2+2M-\frac{1}{\omega^2 C}\right]=0.$$

$$f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{(L_1+L_2+2M)C}}$$

$$\left[(L_2+M)(1+h_{fe})-\frac{1}{\omega_0^2 C}\right]=0$$

$$\boxed{h_{fe} = \frac{L_1+M}{L_2+M}}$$

Colpitt's Oscillator:




→ When the supply voltage $V_{cc}$ is switched ON, a transient current is produced in the tank circuit and then, damped harmonic oscillations are set up in the circuit.

→ This current will produce ac voltage across $C_1$ & $C_2$.

→ As 3 is earthed, it will be at zero potential.

→ If 1 is at positive terminal with respect to 3 at any instant, terminal 2 will be at negative potential with respect to 3 at the same instant. Thus the phase difference between 1 & 2 will be 180°.

→ The frequency of oscillation is

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

$$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2}$$

$$C = \frac{C_1 C_2}{C_1 + C_2}$$

Analysis:

$$Z_1 = \frac{1}{j\omega C_1} = -\frac{j}{\omega C_1}$$

$$Z_2 = \frac{1}{j\omega C_2} = -\frac{j}{\omega C_2}$$

$$Z_3 = j\omega L$$

$$\Rightarrow -j h_{ie}\left(\frac{1}{\omega C_1} + \frac{1}{\omega C_2} - \omega L\right) + \left(\frac{1 + h_{fe}}{\omega^2 C_1 C_2} - \frac{L}{C}\right) = 0$$

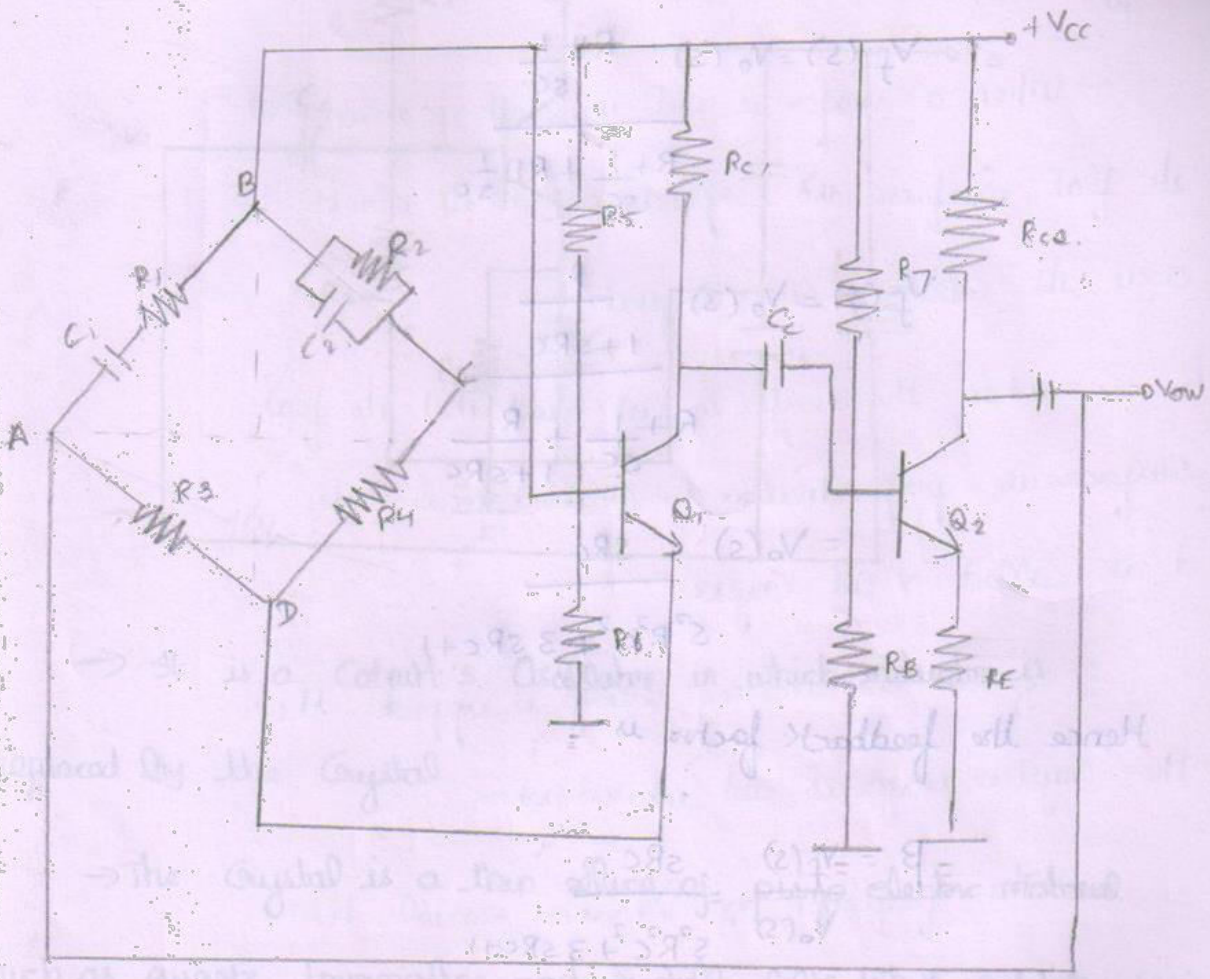
$$f_o = \frac{\omega_o}{2\pi} = \frac{1}{2\pi}\sqrt{\frac{C_1 + C_2}{L C_1 C_2}}$$

$$\boxed{h_{fe} = \frac{C_2}{C_1}}$$

Wien-bridge Oscillator:

→ The Circuit Consist of a two stage RC coupled amplifier which provides a phase shift of 360° (or) 0°.

→ The feedback network consist of lead lag network and a voltage divider.




→ If the bridge is balanced.

$$\frac{R_3}{R_4} = \frac{R_1 - jX_{C_1}}{\left[\frac{R_2(-jX_{C_2})}{R_2 - jX_{C_2}}\right]}$$

$$f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

$$= \frac{1}{2\pi RC} \quad \text{if } R_1 = R_2 = R \text{ and } C_1 = C_2 = C.$$

→ To determine the gain of Wien bridge.

Assume that $R_1 = R_2 = R$

$C_1 = C_2 = C$

$$V_f(s) = V_o(s) \frac{R \| \frac{1}{sC}}{R + \frac{1}{sC} + R \| \frac{1}{sC}}$$

$$V_f(s) = V_o(s) \frac{\frac{R}{1+sRC}}{R + \frac{1}{sC} + \frac{R}{1+sRC}}$$

$$= V_o(s) \frac{sRC}{s^2R^2C^2 + 3sRC + 1}$$

Hence the feedback factor is

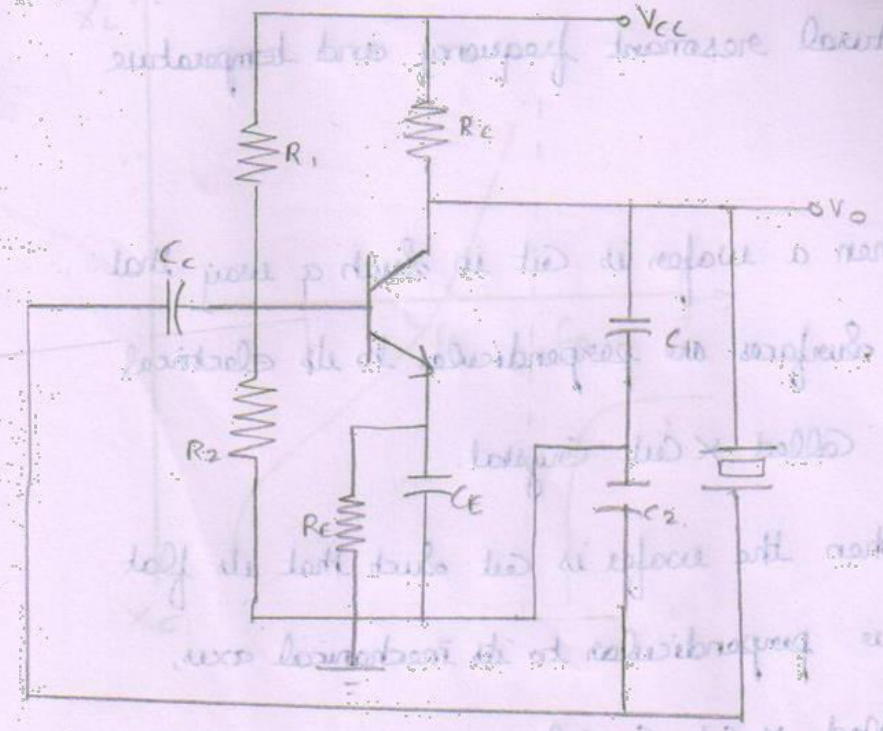
$$\beta = \frac{V_f(s)}{V_o(s)} = \frac{sRC}{s^2R^2C^2 + 3sRC + 1}$$

$A\beta = 1$

The gain of the amplifier is

$$A = \frac{1}{\beta} = \frac{s^2R^2C^2 + 3sRC + 1}{sRC}$$

Crystal Oscillator:




→ It is a Colpitt's Oscillator in which inductor is replaced by the Crystal.

→ The Crystal is a thin slice of piezo electric material such as quartz, tourmaline and rochelle salts which exhibits a property called piezo electric effect.

→ In order to obtain high degree of frequency stability Crystal Oscillator are used.

→ The Crystal is the ground wafer of translucent quartz placed between two metal plates and housed in a stamp sized package.

→ The method of cutting the crystal determines the natural resonant frequency and temperature coefficient.

→ When a wafer is cut in such a way that its flat surfaces are perpendicular to its electrical axis, its called X Cut Crystal.

→ When the wafer is cut such that its flat surfaces are perpendicular to its mechanical axis, it is called Y Cut Crystal.

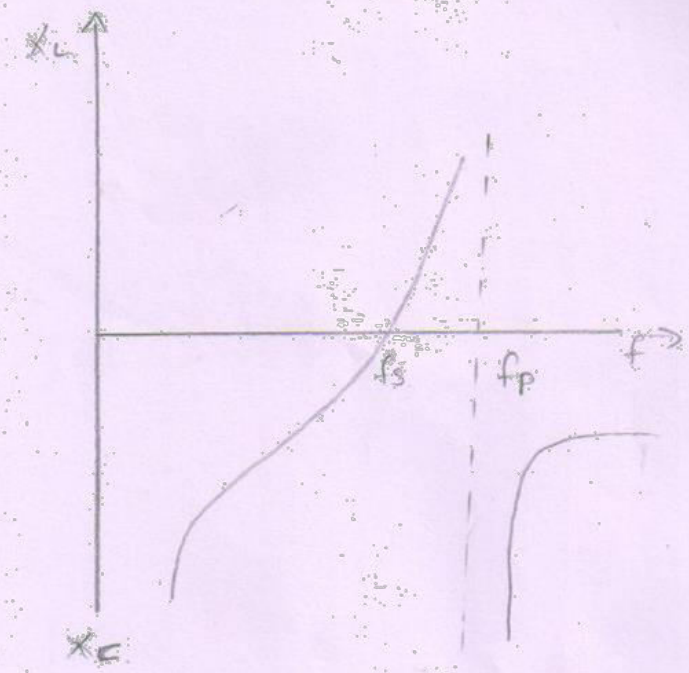
→ If an alternating voltage is applied, then the crystal wafer is set into vibration.

→ The frequency of vibration equal to resonant frequency of the crystal is determined by its characteristics.

$$f = \frac{1}{2l}\sqrt{\frac{Y}{\rho}}$$

Y → young modulus

ρ → density of the material




$$jX = \frac{1}{j\omega C_p} \cdot \frac{\omega^2 - \omega_s^2}{\omega^2 - \omega_p^2}$$

Here, $\omega_s^2 = \frac{1}{LC_s}$

$$\omega_p^2 = \frac{1}{L\left(\frac{1}{C_s} + \frac{1}{C_p}\right)}$$

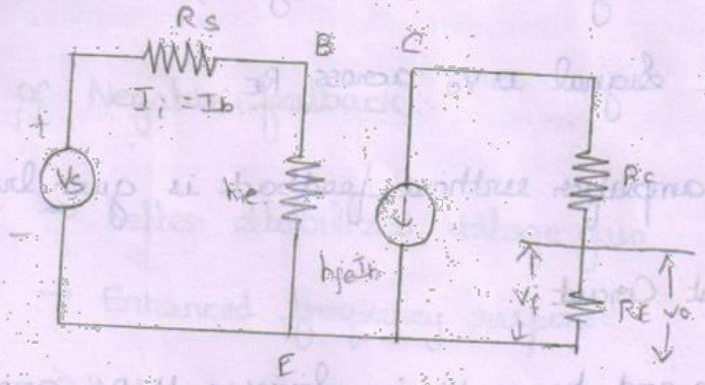
→ The advantages are

→ has high Q as a resonat Circuit

→ Good frequency stability.

Unit V

Completed
29-11-2017




→ $V_f$ & $V_o$ are equal and hence $\beta = V_f/V_o = 1$. This topology stabilises the voltage gain

→ Since $R_s$ is considered as a part of the amplifier then $V_i = V_s$ and the voltage gain without feedback is given by,

$$A_V = \frac{V_o}{V_i} = \frac{h_{fe} I_b R_E}{V_s} = \frac{h_{fe} R_E}{R_s + h_{ie}}$$

where $V_s = I_b (R_s + h_{ie})$

→ The desensitivity is given by,

$$D = 1 + \beta A_V = 1 + \frac{h_{fe} R_E}{R_s + h_{ie}} = \frac{R_s + h_{ie} + h_{fe} R_E}{R_s + h_{ie}}.$$

where $\beta = \frac{V_f}{V_o} = 1$.