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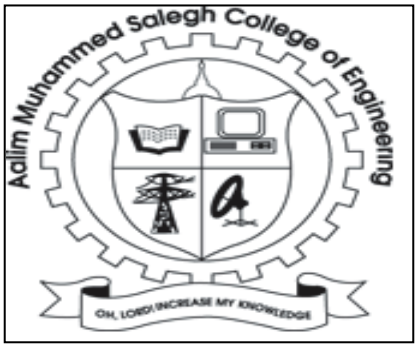


DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

QUESTION BANK

EC8353 ELECTRON DEVICES AND CIRCUITS

Year/Semester: II/III

Regulation – 2017
Academic Year 2019 – 2020

UNIT - 1

PN JUNCTION DEVICES

PART - A

1. Differentiate between Zener Breakdown and Avalanche breakdown. (April/May 2017)

Zener Breakdown

1.The temperature coefficient is negative.

2. This occurs for zener diodes with V_z less than 6V.

Avalanche Breakdown

1. The temperature coefficient is Positive.

2. This occurs for zener diodes with V_z greater than 6V.

2. Mention some of the applications of laser diode. (April/May 2017)

- CD players
- Optical discs
- Laser printers
- Fiber and broad band communication
- Aerospace
- Medical and defence industries

3. State few applications of zener diode. (Nov/Dec 2016)

- As voltage regulators
- As a fixed reference voltage in a network for biasing and comparison purposes and for calibrating voltmeters
- As peak clippers
- For meter protection against damage from accidental application of excessive voltage.

4. Define Rectifiers. List the types of Rectifiers. (Nov/Dec 2016)

An electrical device which converts an alternating current into a direct one by allowing a current to flow through it in one direction only.

Types of rectifier:

- Half wave rectifier
- Full wave rectifier
- Bridge rectifier

5. Define Semiconductor.

A semiconductor is a substance, usually a solid chemical element or compound, that can conduct electricity under some conditions but not others, making it a good medium for the control of electrical current.

6. Classify Semiconductors.

- Intrinsic semiconductor(pure)
- Extrinsic semiconductor(impure)
    - n-type
    - p-type

7. Define Hole Current.

Current due to hole carriers in any semiconductor is called as hole current.

8. Define Knee voltage of a Diode.

The minimum voltage at which the diode starts conducting and current starts increasing Exponentially is called knee voltage of a diode.

9. What is Peak Inverse Voltage?

In reverse biased, opposite polarity voltage appears across diode. The maximum voltage which diode can withstand without breakdown is called peak inverse voltage.

10. Define Depletion Region in PN Junction Diode.

The region which is free of mobile charge carriers is called as depletion region.

11. What is Barrier Potential?

Under reverse bias condition of PN junction, potential barrier will be formed. It prevents the flow of majority carriers in both directions.

12. Define Reverse Saturation Current in PN Junction Diode.

Under reverse bias condition, thermally generated holes in the P region attracted towards the negative terminal of the battery and the electrons in the N region attracted towards the positive terminal of the battery. Consequently, the minority carriers, electrons in the P region and holes in the N region, wander over to the junction and flow towards their majority carrier side giving rise to small reverse current known as reverse saturation current.

13. What is meant by Diffusion Current in a Semi-conductor?

Diffusion current is a current in a semiconductor caused by the diffusion of charge carriers (holes and/or electrons).

14. What is meant by drift current?

Drift current is due to the motion of charge carriers due to the force exerted on them by an electric field.

15. Differentiate diffusion current and drift current.

Diffusion current	Drift current
Diffusion current may occur even if there isn't an electric field in the semiconductor.	Drift current requires an the electric field to be present.
The magnitude of the diffusion current depends on the slope of the carrier concentration, and not the concentration itself.	The magnitude depends on the carrier concentration.
Direction of the diffusion current depends on the slope of the carrier concentration, and not the concentration itself.	Direction of the drift current is always in the direction of the electric field.
Does not obey Ohm's law	Obeys Ohm's law

16. What is meant by dynamic resistance of diode?

The resistance offered by the p-n junction diode under A.C condtions is called dynamic resistance of diode.

17. Compare the various types of Rectifiers.

Particulars	Half-wave	Full-wave	Bridge
No. of diodes	1	2	4
Maximum efficiency	40.6%	81.2%	81.2%
Ripple factor	1.21	0.48	0.48
Peak inverse voltage	V_m	$2V_m$	V_m
Output frequency	f	2f	2f
Transformer utilization factor	0.287	0.693	0.812
Form factor	1.57	1.11	1.11
Peak factor	2	$\sqrt{2}$	$\sqrt{2}$

18. Define Voltage Regulators. List the types of Voltage Regulators.

A voltage regulator is an electronic circuit that provides a stable d.c voltage independent of the load current, temperature and a.c line voltage variations.

Types of regulator are series regulator and shunt regulator.

19. Compare series and shunt regulator.

Shunt regulator	Series regulator
1. The control element is in parallel with the load	The control element is in series with the load
2. Only small current passes through the control element, which is required to be diverted to keep output constant.	The entire load current is always passes through the control element.

20. Define Electroluminescence.

Electroluminescence (**EL**) is an optical phenomenon and electrical phenomenonin which a material emits light in response to the passage of an electric current or to a strong electric field. This is distinct from black body light emission resulting from heat (incandescence), from a chemical reaction (chemiluminescence), sound (sonoluminescence), or other mechanical action (mechanoluminescence).

21. What are the advantages and limitations of LCD Displays?

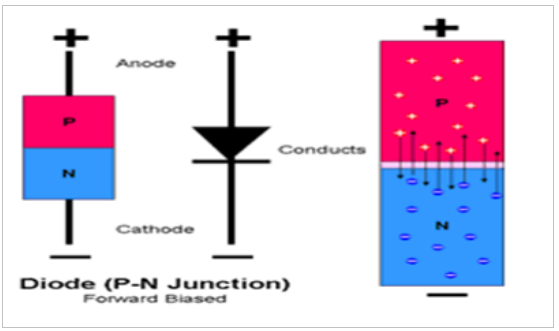
- Less power consumption is the advantage of LCD displays.
- Poor reliability is the limitation of LCD Display.

22. What is transition capacitance

During reverse bias, the minority carriers move away from the junction, thereby having uncovered immobile carriers on either side of the junction. Hence the thickness of the space charge layer at the junction increases with reverse voltage. This increase in uncovered charge with applied voltage may be considered as a capacitive effect called as transition capacitance.

23. What is PN junction diode?

There are two electrodes each from p-type and n-type materials and due to these two electrodes; the device is called a diode. It conducts only in one direction.



24. What are the advantages of bridge rectifier over its centre tapped counterpart?

- No centre tap is required in the transformer secondary. Hence, wherever possible a.c Voltage can be directly applied to the bridge.
- Due to pure alternating current in secondary of transformer, the transformer gets utilized effectively.

25. What is LED? Draw its symbol.

LED is a light emitting diode which emits light when forward biased.

26. Define static and dynamic resistance of a PN diode.

The forward resistance of p-n junction diode when p-n junction is used in D.C circuit and the applied forward voltage is d.c. is called static resistance The resistance offered by the p-n junction diode under a.c. conditions is called dynamic Resistance of diode.

PART-B

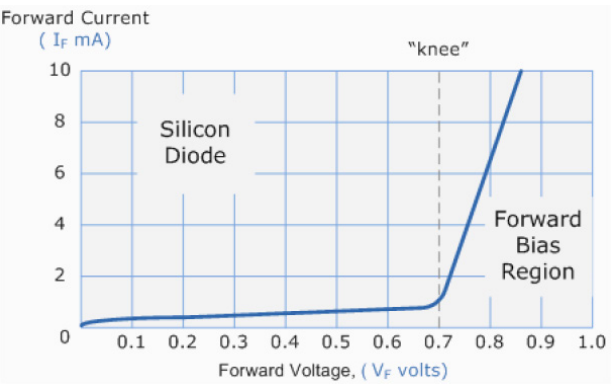
1. With a neat diagram explain the working of a PN junction diode in forward bias and reverse bias and show the effect of temperature on its V-I characteristics. (16)

(Nov/Dec 2015, Nov/Dec 2014, May/June 2014, Nov/Dec 2013, Nov/Dec 2012)

Solution:

FORWARD BIASED JUNCTION DIODE

When a diode is connected in a Forward Bias condition, a negative voltage is applied to the N type material and a positive voltage is applied to the P-type material. If this external voltage becomes greater than the value of the potential barrier, approx. 0.7 volts for silicon and 0.3 volts for germanium, the potential barriers opposition will be overcome and current will start to flow. This is because the negative voltage pushes or repels electrons towards the junction giving them the energy to cross over and combine with the holes being pushed in the opposite direction towards the junction by the positive voltage. This results in a characteristics curve of zero current flowing up to this voltage point, called the "knee" on the static curves and then a high current flow through the diode with little increase in the external voltage as shown below.

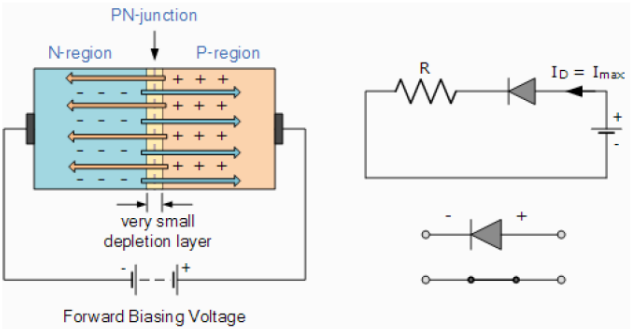


Diode Forward Characteristics

The application of a forward biasing voltage on the junction diode results in the depletion layer becoming very thin and narrow which represents a low impedance path through the junction thereby allowing high currents to flow. The point at which this sudden increase in current

takes place is represented on the static I-V characteristics curve above as the "knee" point.

Forward Biased Junction Diode showing a Reduction in the Depletion Layer



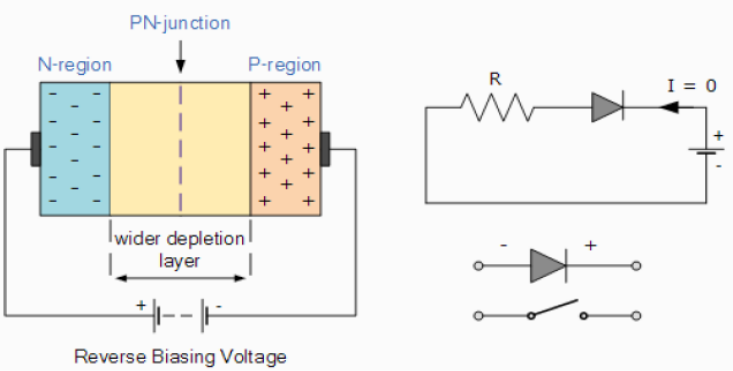
Diode Forward Bias

This condition represents the low resistance path through the PN junction allowing very large currents to flow through the diode with only a small increase in bias voltage. The actual potential difference across the junction or diode is kept constant by the action of the depletion layer at approximately 0.3v for germanium and approximately 0.7v for silicon junction diodes. Since the diode can conduct "infinite" current above this knee point as it effectively becomes a short circuit, therefore resistors are used in series with the diode to limit its current flow. Exceeding its maximum forward current specification causes the device to dissipate more power in the form of heat than it was designed for resulting in a very quick failure of the device.

PN JUNCTION UNDER REVERSE BIAS CONDITION:

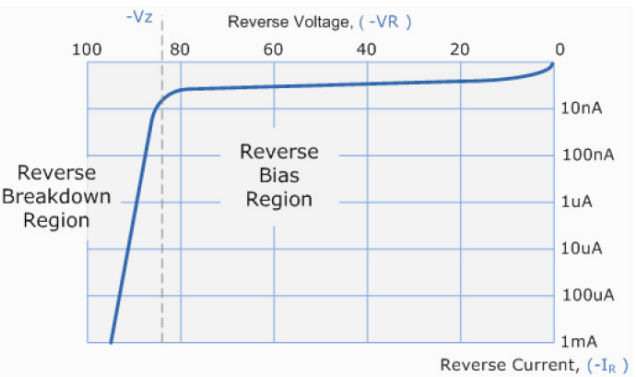
When a diode is connected in a **Reverse Bias** condition, a positive voltage is applied to the N-type material and a negative voltage is applied to the P-type material. The positive voltage applied to the N type material attracts electrons towards the positive electrode and away from the junction, while the holes in the P-type end are also attracted away from the junction towards the negative electrode. The net result is that the depletion layer grows wider due to a lack of electrons and holes and presents a high impedance path, almost an insulator. The result is that a high potential barrier is created thus preventing current from flowing through the semiconductor material.

Reverse Biased Junction Diode showing an Increase in the Depletion



Diode Reverse Bias

This condition represents a high resistance value to the PN junction and practically zero current flows through the junction diode with an increase in bias voltage. However, a very small leakage current does flow through the junction which can be measured in microamperes, (μA). One final point, if the reverse bias voltage V_r applied to the diode is increased to a sufficiently high enough value, it will cause the PN junction to overheat and fail due to the avalanche effect around the junction. This may cause the diode to become shorted and will result in the flow of maximum circuit current, and this shown as a step downward slope in the reverse static characteristics curve below.



Diode Reverse Characteristics

Sometimes this avalanche effect has practical applications in voltage stabilizing circuits where a series limiting resistor is used with the diode to limit this reverse breakdown current to a preset maximum value thereby

producing a fixed voltage output across the diode. These types of diodes are commonly known as **Zener Diodes**

VI CHARACTERISTICS AND THEIR TEMPERATURE DEPENDENCE

Diode terminal characteristics equation for diode junction current:

$$I_D = I_0\left(e^{\frac{v}{nV_T}} - 1\right)$$

Where $V_T = KT/q$;

V_D- diode terminal voltage, volts

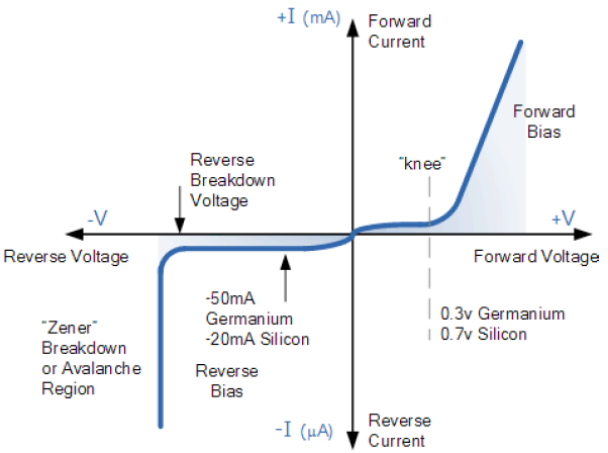
I_0 – temperature-dependent saturation current, μA

T – absolute temperature of p-n junction,K

K – Boltzmann's Constant (1.38×10^{-23}j/K)

Q – electron charge 1.6×10^{-19} C

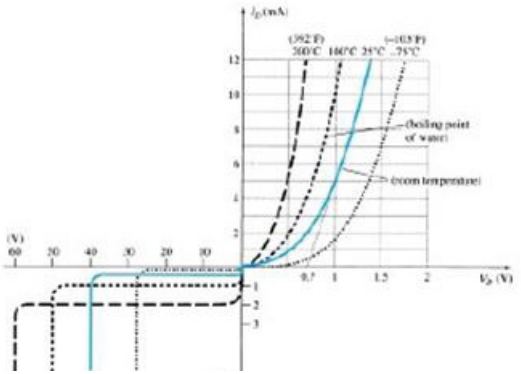
η =empirical constant, 1 for Ge and 2 for Si



Diode Characteristics

Temperature Effects on Diode

Temperature can have a marked effect on the characteristics of a silicon semiconductor diode as shown in figure below. It has been found experimentally that the reverse saturation current Io will just about double in magnitude for every 10°C increase in temperature.



Variation in Diode Characteristics with temperature change

It is not uncommon for a germanium diode with an Io in the order of 1 or 2 A at 25°C to have a leakage current of 100 A - 0.1 mA at a temperature of 100°C. Typical values of Io for silicon are much lower than that of germanium for similar power and current levels. The result is that even at high temperatures the levels of Io for silicon diodes do not reach the same high levels obtained. For germanium—a very important reason that silicon devices enjoy a significantly higher level of development and utilization in design. Fundamentally, the open-circuit equivalent in the reverse bias region is better realized at any temperature with silicon than with germanium. The increasing levels of I_o with temperature account for the lower levels of threshold voltage, as shown in figure. Simply increase the level of I_o in and not rise in diode current. Of course, the level of T°K also will be increase, but the increasing level of I_o will overpower the smaller percent change in T°K. As the temperature increases the forward characteristics are actually becoming more "ideal,"

2. Explain V-I characteristics of Zener diode. (8)

(Nov/Dec 2015, Nov/Dec 2013)

Zener diode

A Zener diode is a type of diode that permits current not only in the forward direction like a normal diode, but also in the reverse direction if the voltage is larger than the breakdown voltage known as "Zener knee voltage" or "Zener voltage". The device was named after Clarence Zener, who discovered this electrical property.

Diode symbol

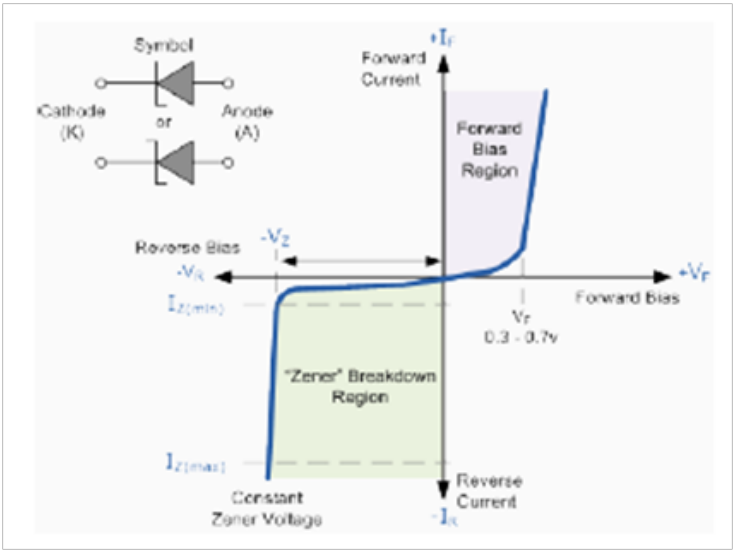
However, the Zener Diode or "Breakdown Diode" as they are sometimes called, are basically the same as the standard PN junction diode but are specially designed to have a low pre-determined Reverse Breakdown Voltage that takes advantage of this high reverse voltage. The point at which a zener diode breaks down or conducts is called the "Zener Voltage" (V_z).

The Zener diode is like a general-purpose signal diode consisting of a silicon PN junction. When biased in the forward direction it behaves just like a normal signal diode passing the rated current, but when a reverse voltage is applied to it the reverse saturation current remains fairly constant over a wide range of voltages. The reverse voltage increases until the diodes breakdown voltage VB is reached at which point a process called Avalanche Breakdown occurs in the depletion layer and the current flowing through the zener diode increases dramatically to the maximum circuit value (which is usually limited by a series resistor). This breakdown voltage point is called the "zener voltage" for zener diodes.

The point at which current flows can be very accurately controlled (to less than 1% tolerance) in the doping stage of the diodes construction giving the diode a specific *zener breakdown voltage*, (V_z) ranging from a few volts up to a few hundred volts. This zener breakdown voltage on the I-V curve is almost a vertical straight line.

Zener diode characteristics

The Zener Diode is used in its "reverse bias" or reverse breakdown mode, i.e. the diodes anode connects to the negative supply. From the I-V characteristics curve above, we can see that the zener diode has a region in its reverse bias characteristics of almost a constant negative voltage regardless of the value of the current flowing through the diode and remains nearly constant even with large changes in current as long as the zener diodes current remains between the breakdown current $I_{Z(min)}$ and the maximum current rating $I_{Z(max)}$.



3. Explain the operation of FWR with centre tap transformer. Also derive its performance parameters. (16)

(Apr/May 2015, Nov/Dec 2013)

A full-wave rectifier converts an ac voltage into a pulsating dc voltage using both half cycles of the applied ac voltage. In order to rectify both the half cycles of ac input, two diodes are used in this circuit. The diodes feed a common load RL with the help of a center-tap transformer. A center-tap transformer is the one, which produces two sinusoidal waveforms of same magnitude and frequency but out of phase with respect to the ground in the secondary winding of the transformer. The full wave rectifier is shown in the **fig 4** below

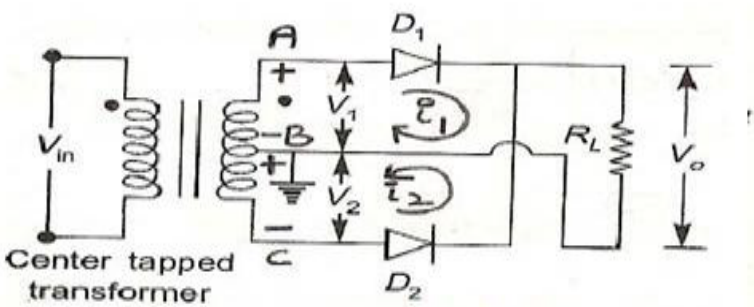


fig 4 Full-Wave Rectifier

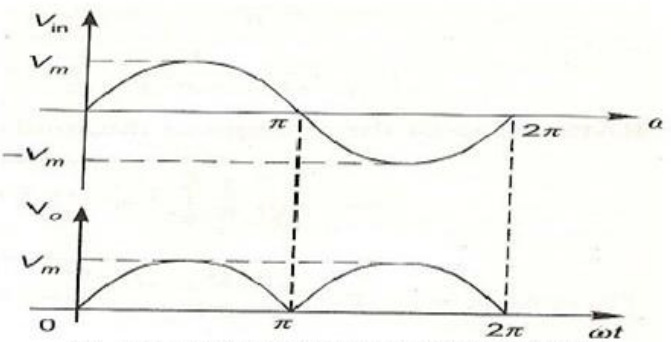


Fig. 5 input and output waveforms of Fullwave rectifier

Fig. 5 shows the input and output wave forms of the ckt.

During positive half of the input signal, anode of diode D_1 becomes positive and at the same time the anode of diode D_2 becomes negative. Hence D_1 conducts and D_2 does not conduct. The load current flows through D_1 and the voltage drop across RL will be equal to the input voltage. During the negative half cycle of the input, the anode of D_1 becomes negative and the anode of D_2 becomes positive. Hence, D_1 does not conduct and D_2 conducts. The load current flows through D_2 and the voltage drop across RL will be equal to the input voltage. It is noted that the load current flows in the both the half cycles of ac voltage and in the same direction through the load resistance.

i) AVERAGEVOLTAGE

$$V_{dc} = I_{dc}.R_{L}. = \frac{21_m}{\pi} = R_t \quad \text{we know } I_m = \frac{V_m}{R_S + R_f + R_L}$$

$$\therefore V_{dc} = \frac{2.V_m R_L}{\pi(R_S + R_f + R_L)}$$

$$\text{If } (R_S + R_f) << R_L$$

$$V_{dc} = \frac{2V_m}{\pi} = 0.637\, V_m.$$

ii) AVERAGE CURRENT

$$\frac{1}{2\pi}\int_0^{L\pi} id\theta = \frac{1}{2\pi}\int_0^{L\pi} I_m \sin\theta\, d\theta$$

$$I_{dc} = \frac{I_m}{2\pi}\left[\int_0^{\pi} \sin\theta d\theta - \int_{\pi}^{2\pi} \sin\theta d\theta\right]$$

$$= \frac{I_m}{2\pi}\left[(-2)(-2)\right]$$

$$= \frac{I_m}{2\pi}.4 = \frac{2I_m}{\pi} = 0.637I_m$$

$$\boxed{I_{dc} = 0.637I_m.}$$

$$\therefore I_{DC}\ \text{FWR} = 2I_{DC}\ \text{HWR}.$$

iii) RMS VOLTAGE:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2 d(Wt)}$$

$$V_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} \left(V_m \sin(wt)\right)^2 d(wt)}$$

$$\boxed{V_{rms} = \frac{V_m}{\sqrt{2}}}$$

IV) RMS CURRENT

$$\boxed{I_{rms} = \frac{2I_m}{\pi}}$$

V) PEAK FACTOR

$$\text{Peak factor} = \frac{\text{peakvalue}}{\text{rmsvalue}}$$

$$\text{Peak Factor} = \frac{V_m}{(V_m/2)}$$

$$\text{Peak Factor} = 2$$

vi) Form Factor

$$\text{Form factor} = \frac{\text{Rms value}}{\text{average value}}$$

$$\text{Form factor} = \frac{\left(V_m/\sqrt{2}\right)}{2V_m/\pi}$$

$$\text{Form factor} = 1.11$$

vii) RIPPLE FACTOR

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

for FWR.

$$I_{rms} = \frac{I_m}{\sqrt{2}} \& I_{DC} = \frac{2I_m}{\pi}$$

$$\therefore \gamma_{FWR} = \sqrt{\left(\frac{I_m}{\sqrt{2}} / \frac{2I_m}{\pi}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{3.1416}{2 \times 1.414}\right)^2 - 1} = 0.483$$

viii) Efficiency (η):

$$\eta = \frac{0/\text{ppower}}{i/\text{ppower}} * 100$$

$$\eta = \frac{p_{dc}}{p_{ac}} \times 100\%$$

$$\text{For FWR}, p_{dc} = I^2_{dc}.R_L = \left(\frac{2}{\pi}.I_m\right)^2.R_L$$

$$P_{ac} = I^2_{rms}\left(R_f + R_S + R_L\right)$$

$$\left(\frac{I_m}{\sqrt{2}}\right)^2\left(R_f + R_S + R_L\right)$$

$$\eta = \frac{\frac{I^2_m 4}{\pi^2}.R_L}{\frac{I^2 m^2}{2}.\left(R_f + R_S + R_L\right)}$$

$$\text{If}\left(R_f + R_S\right) << R_L$$

$$\eta = \frac{4}{\pi^2}.\frac{2}{1} = \frac{8}{\pi^2} = 0.812 = 81.2\%$$

ix) Transformer Utilization Factor (TUF):

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the transformer used in the circuit. So, transformer utilization factor is defined as

$$TUF = \frac{P_{dc}}{P_{ac(rated)}}$$

a) $TUF(\text{sec ondary}) = \dfrac{P_{dc} \text{ delivered to load}}{\text{AC power rating of transformer sec ondary}}$

b) Since both the windings are used $TUF_{FWR} = 2TUF_{FWR}$

$= \quad 2 \times 0.287 = 0.574$

c) TUF primary = Rated efficiency $= \dfrac{P_{dc}}{P_{ac}} \times 100 = 81.2\%$

d) Average $= \dfrac{0.812 + 0.574}{2} = 0.693$

x) Peak Inverse Voltage (PIV):

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. The peak inverse voltage across a diode is the peak of the negative half- cycle. For half- wave rectifier, PIV is $2V_m$

xi) % Regulation:

$$\text{Voltage regulation} = \frac{I_{dc}(R_S + R_f)}{\frac{2V_m}{\pi} - I_{DC}(R_f + R_S)}$$

Advantages

1) Ripple factor = 0.482 (against 1.21 for HWR)

2) Rectification efficiency is 0.812 (against 0.405 for HWR)

3) Better TUF (secondary) is 0.574 (0.287 for HWR)

4) No core saturation problem

Disadvantages:

1) Requires center tapped transformer.

4. Explain the working of bridge rectifier. Give the expression for RMS current, PIV, ripple factor and efficiency.

(April/May2017, Nov/Dec2014, May/June 2014)

Another type of circuit that produces the same output waveform as the full wave rectifier circuit is **Full Wave Bridge Rectifier**. This type of single phase rectifier uses four individual rectifying diodes connected in

a closed loop "bridge" configuration to produce the desired output. The main advantage of this bridge circuit is that it does not require a special centre tapped transformer, thereby reducing its size and cost. The single secondary winding is connected to one side of the diode bridge network and the load to the other side as shown below.

The Diode Bridge Rectifier

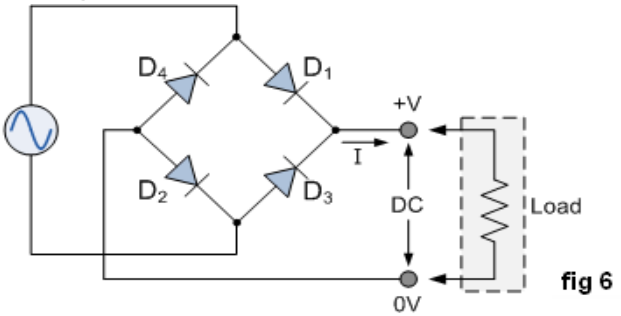


fig 6

The four diodes labelled D_1 to D_4 are arranged in "series pairs" with only two diodes conducting current during each half cycle. During the positive half cycle of the supply, diodes D_1 and D_2 conduct in series while diodes D_3 and D_4 are reverse biased and the current flows through the load as shown below (fig 7).

The Positive Half-cycle

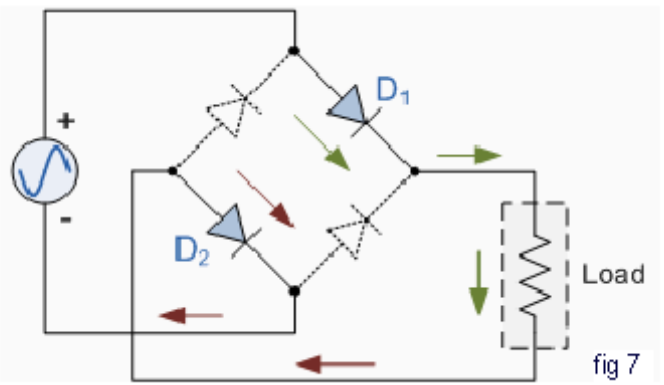


fig 7

The Negative Half-cycle

During the negative half cycle of the supply, diodes D_3 and D_4 conduct in series (fig 8), but diodes D_1 and D_2 switch "OFF" as they are now reverse biased. The current flowing through the load is the same direction as before.

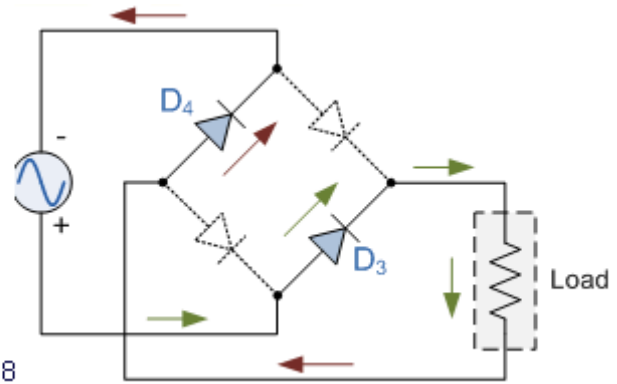


fig 8

As the current flowing through the load is unidirectional, so the voltage developed across the load is also unidirectional the same as for the previous two diode full-wave rectifier, therefore the average DC voltage across the load is $0.637V_{max}$. However in reality, during each half cycle the current flows through two diodes instead of just one so the amplitude of the output voltage is two voltage drops (2 x 0.7 = 1.4V) less than the input V_{max} amplitude. The ripple frequency is now twice the supply frequency (e.g. 100Hz for a 50Hz supply)

Therefore, the following expressions are same as that of full wave refctifier.

a) Average current $I_{dc} = \frac{2I_m}{\pi}$

b) RMS current $I_{rms} = \frac{I_m}{\sqrt{2}}$

c) DC output voltage (no, load) $V_{DC} \frac{2V_m}{\pi}$

d) Ripple factor $\gamma = 0.482$

e) Rectification efficiency $= \eta = 0.812$

f) DC output voltage full load,

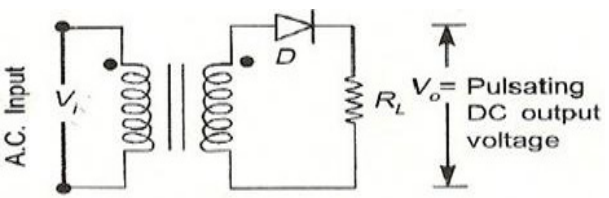
$$= V_{DCM} = \frac{2V_m}{\pi} - I_{dc}\left(R_s + 2R_f\right); \qquad \text{i.e. less by one diode loss.}$$

TUF of both primary & secondary are 0.812 therefore TUF overall is 0.812 (better than FWR with 0.693)

S.No	Parameter	HWR	FWR	BR
1.	No of diodes	1	2	4
2	PIV of diodes	V_m	$2\,V_m$	V_m
3	Secondary voltage (rms)	V	V-0-V	V
4	DC output at no load	$\frac{V_m}{\pi} = 0.318\,V_m$	$\frac{2V_m}{\pi} = 0.36\,V_m$	$\frac{2V_m}{\pi} = 0.636\,V_m$
5	Ripple factor γ	1.21	0.482	0.0482
6	Ripple frequency	f	2f	2f
7	Rectification efficiency η	0.406	0.812	0.812
8	TUF	0.287	0.693	0.812

5. With neat diagram explain the circuit operation of half wave rectifier. (Nov/Dec 2016, Nov/Dec 2015)

A Half – wave rectifier as shown in fig 1.2 is one, which converts a.c. voltage into a pulsating voltage using only one half cycle of the applied a.c. voltage.



Basic structure of Half-Wave Rectifier

The a.c. voltage is applied to the rectifier circuit using step-down transformer-rectifying element i.e., pn junction diode and the source of a.c. voltage, all connected is series. The a.c. voltage is applied to the rectifier circuit using step-down transformer

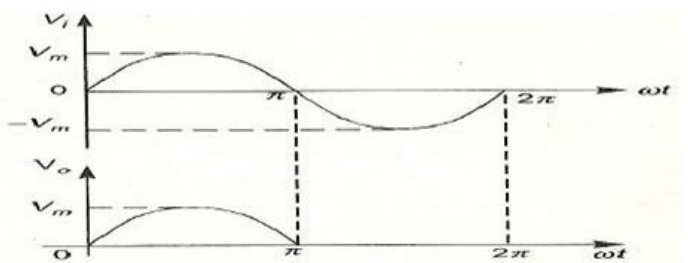


fig 3 Input and output waveforms of a Half wave rectifier

$V=V_m \sin(wt)$

The input to the rectifier circuit, Where V_m is the peak value of secondary a.c. voltage.

Operation:

For the positive half-cycle of input a.c. voltage, the diode D is forward biased and hence it conducts. Now a current flows in the circuit and there is a voltage drop across RL. The waveform of the diode current (or) load current is shown in **fig 3**.

For the negative half-cycle of input, the diode D is reverse biased and hence it does not

Conduct. Now no current flows in the circuit i.e., i=0 and V_o=0. Thus for the negative half- cycle no power is delivered to the load.

Analysis:

In the analysis of a HWR, the following parameters are to be analyzed.

1. DC output current
2. DC Output voltage
3. R.M.S. Current
4. R.M.S. voltage
5. Rectifier Efficiency (η)
6. Ripple factor (γ)
7. Peak Factor
8. % Regulation
9. Transformer Utilization Factor (TUF)
10. form factor
11. o/p frequency

Let a sinusoidal voltage V_i be applied to the input of the rectifier. Then $V=V_m \sin(wt)$ Where V_m is the maximum value of the secondary voltage. Let the diode be idealized to piece-wise linear approximation with resistance R_f in the forward direction i.e., in the ON state and R_r ($=\infty$) in the reverse direction i.e., in the OFF state. Now the current 'i' in the diode (or) in the load resistance RL is given by $V=V_m \sin(wt)$

i) AVERAGE VOLTAGE

$$V_{dc} = \frac{1}{T}\int_0^T V\, d(wt)$$

$$V_{dc} = \frac{1}{T}\int_0^{2\pi} V(a)\, da$$

$$V_{dc} = \frac{1}{2\pi}\int_{\pi}^{2\pi} V(a)\, da$$

$$V_{dc} = \frac{1}{2\pi}\int_0 V_m \sin(wt)$$

$$V_{dc} = \frac{V_m}{\pi}$$

ii).AVERAGE CURRENT:

$$I_{dc} = \frac{I_m}{\pi}$$

iii) RMS VOLTAGE:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2 d(wt)}$$

$$V_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} \left(v_m \sin(wt)\right)^2 d(wt)}$$

$$\boxed{V_{rms} = \frac{V_m}{2}}$$

IV) RMS CURRENT

$$\boxed{I_{rms} = \frac{2I_m}{\pi}}$$

V) PEAK FACTOR

$$\text{Peak folder} = \frac{\text{peakvalue}}{\text{rmsvalue}}$$

$$\text{Peak factor} = \frac{V_m}{(V_m/2)}$$

$$\text{Peak factor} = 2$$

VI) FORM FACTOR

$$\text{Form factor} = \frac{\text{Rms value}}{\text{average value}}$$

$$\text{Form factor} = \frac{(V_m / 2)}{V_m / \pi}$$

$$\text{Form factor} = 1.57$$

VII) RIPPLE FACTOR

$$r = \frac{V_{ac}}{V_{dc}}$$

$$V_{ac} = \sqrt{V^2_{rms} - V^2_{dc}}$$

$$r = \sqrt{\frac{V^2_{rms} - V^2_{dc}}{V_{ac}}}$$

$$r = \sqrt{\frac{V^2_{rms}}{V^2_{dc}} - 1}$$

$$r = 1.21$$

Viii) Efficiency (η):

$$\eta = \frac{0 / \text{ppower}}{i / \text{ppower}} * 100$$

$$\eta = \frac{P_{ac}}{P_{dc}} * 100$$

$$\eta = 40.8$$

ix) Transformer Utilization Factor (TUF):

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the transformer used in the circuit. Therefore, transformer utilization factor is defined as

$$TUF = \frac{P_{dc}}{P_{ac(rated)}}$$

$$TUF = 0.286$$

The value of TUF is low which shows that in half-wave circuit, the transformer is not fully utilized. If the transformer rating is 1 KVA

(1000VA) then the half-wave rectifier can deliver 1000 X 0.287 = 287 watts to resistance load.

x) Peak Inverse Voltage (PIV):

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. The peak inverse voltage across a diode is the peak of the negative half- cycle. For half-wave rectifier, PIV is V_m.

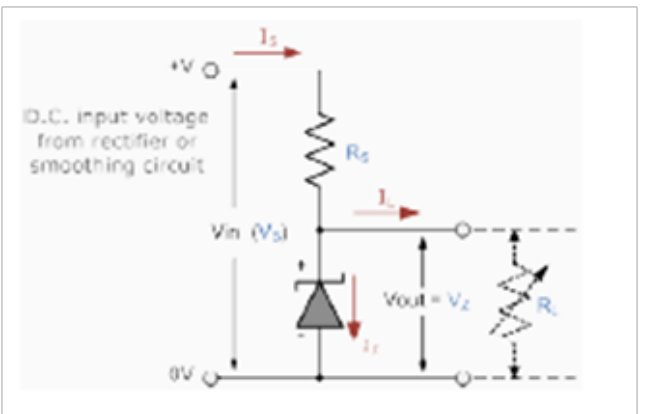
DISADVANTAGES OF HALF-WAVE RECTIFIER:

1. The ripple factor is high.
2. The efficiency is low.
3. The Transformer Utilization factor is low.

Because of all these disadvantages, the half-wave rectifier circuit is normally not used as a power rectifier circuit.

6. Why the Zener diode is called as regulator (8)
(April/May 2017, Apr/May2015, May/June 2014)

The Zener Diode Regulator



Zener Diodes can be used to produce a stabilised voltage output with low ripple under varying load current conditions. By passing a small current through the diode from a voltage source, via a suitable current limiting resistor (R_S), the zener diode will conduct sufficient current to maintain a voltage drop of V_{out}. We remember from the previous tutorials that the DC output voltage from the half or full-wave rectifiers contains ripple superimposed onto the DC voltage and that as the load value changes so to does the average output voltage. By connecting a simple zener stabiliser

circuit as shown below across the output of the rectifier, a more stable output voltage can be produced.

7. Explain in detail about LASER diode. (APR/MAY2015)

Laser diode:

A laser diode, or LD, is an electrically pumped semiconductor laser in which the active medium is formed by a p-n junction of a semiconductor diode similar to that found in a light-emitting diode.The laser diode is the most common type of laser produced. Laser diodes have a very wide range of uses that include, but are not limited to, fiber optic communications, barcode readers, laser pointers, CD/DVD/Blu-ray reading, laser printing, scanning and increasingly directional lighting sources.

A laser diode is electrically a P-i-n diode. The active region of the laser diode is in the intrinsic (I) region, and the carriers, electrons and holes, are pumped into it from the N and P regions respectively. While initial diode laser research was conducted on simple P-N diodes, all modern lasers use the double-heterostructure implementation, where the carriers and the photons are confined in order to maximize their chances for recombination and light generation. Unlike a regular diode used in electronics, the goal for a laser diode is that all carriers recombine in the I region, and produce light. Thus, laser diodes are fabricated using direct bandgap semiconductors. The laser diode epitaxial structure is grown using one of the crystal growth techniques, usually starting from an N doped substrate, and growing the I doped active layer, followed by the P doped cladding, and a contact layer. The active layer most often consists of quantum wells, which provide lower threshold current and higher efficiency.

Laser diodes form a subset of the larger classification of semiconductor p-n junction diodes. Forward electrical bias across the laser diode causes the two species of charge carrier – holes and electrons – to be "injected" from opposite sides of the p-n junction into the depletion region. Holes are injected from the p-doped, and electrons from the n-doped, semiconductor. (A depletion region, devoid of any charge carriers, forms as a result of the difference in electrical potential between n- and p-type semiconductors wherever they are in physical contact.) Due to the use of charge injection in powering most diode lasers, this class of lasers is sometimes termed "injection lasers," or "injection laser diode" (ILD). As diode lasers are semiconductor devices, they may also be classified as semiconductor

lasers. Either designation distinguishes diode lasers from solid-state lasers.

Another method of powering some diode lasers is the use of optical pumping. Optically pumped semiconductor lasers (OPSL) use a III-V semiconductor chip as the gain medium, and another laser (often another diode laser) as the pump source. OPSL offer several advantages over ILDs, particularly in wavelength selection and lack of interference from internal electrode structures.

When an electron and a hole are present in the same region, they may recombine or "annihilate" with the result being spontaneous emission — i.e., the electron may re-occupy the energy state of the hole, emitting a photon with energy equal to the difference between the electron and hole states involved. (In a conventional semiconductor junction diode, the energy released from the recombination of electrons and holes is carried away as phonons, i.e., lattice vibrations, rather than as photons.) Spontaneous emission gives the laser diode below lasing threshold similar properties to an LED. Spontaneous emission is necessary to initiate laser oscillation, but it is one among several sources of inefficiency once the laser is oscillating.

The difference between the photon-emitting semiconductor laser and conventional phonon- emitting (non-light-emitting) semiconductor junction diodes lies in the use of a different type of semiconductor, one whose physical and atomic structure confers the possibility for photon emission. These photon-emitting semiconductors are the so-called "direct bandgap" semiconductors. The properties of silicon and germanium, which are single-element semiconductors, have bandgaps that do not align in the way needed to allow photon emission and are not considered "direct." Other materials, the so-called compound semiconductors, have virtually identical crystalline structures as silicon or germanium but use alternating arrangements of two different atomic species in a checkerboard-like pattern to break the symmetry. The transition between the materials in the alternating pattern creates the critical "direct bandgap" property. Gallium arsenide, indium phosphide, gallium antimonide, and gallium nitride are all examples of compound semiconductor materials that can be used to create junction diodes that emit light.

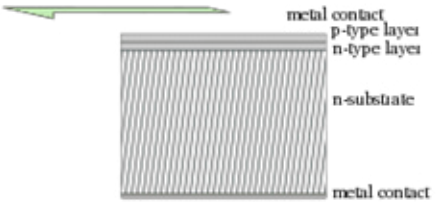


Diagram of a simple laser diode, such as shown above; not to scale

In the absence of stimulated emission (e.g., lasing) conditions, electrons and holes may coexist in proximity to one another, without recombining, for a certain time, termed the "upper-state lifetime" or "recombination time" (about a nanosecond for typical diode laser materials), before they recombine. Then a nearby photon with energy equal to the recombination energy can cause recombination by stimulated emission. This generates another photon of the same frequency, travelling in the same direction, with the same polarization and phase as the first photon. This means that stimulated emission causes gain in an optical wave (of the correct wavelength) in the injection region, and the gain increases as the number of electrons and holes injected across the junction increases. The spontaneous and stimulated emission processes are vastly more efficient in direct bandgap semiconductors than in indirect bandgap semiconductors; therefore silicon is not a common material for laser diodes.

As in other lasers, the gain region is surrounded with an optical cavity to form a laser. In the simplest form of laser diode, an optical waveguide is made on that crystal surface, such that the light is confined to a relatively narrow line. The two ends of the crystal are cleaved to form perfectly smooth, parallel edges, forming a Fabry–Pérot resonator. Photons emitted into a mode of the waveguide will travel along the waveguide and be reflected several times from each end face before they are emitted. As a light wave passes through the cavity, it is amplified by stimulated emission, but light is also lost due to absorption and by incomplete reflection from the end facets. Finally, if there is more amplification than loss, the diode begins to "lase".

Some important properties of laser diodes are determined by the geometry of the optical cavity. Generally, in the vertical direction, the light is contained in a very thin layer, and the structure supports only a single

optical mode in the direction perpendicular to the layers. In the transverse direction, if the waveguide is wide compared to the wavelength of light, then the waveguide can support multiple transverse optical modes, and the laser is known as "multi-mode". These transversely multi-mode lasers are adequate in cases where one needs a very large amount of power, but not a small diffraction-limited beam; for example in printing, activating chemicals, or pumping other types of lasers.

In applications where a small focused beam is needed, the waveguide must be made narrow, on the order of the optical wavelength. This way, only a single transverse mode is supported and one ends up with a diffraction-limited beam. Such single spatial mode devices are used for optical storage, laser pointers, and fiber optics. Note that these lasers may still support multiple longitudinal modes, and thus can lase at multiple wavelengths simultaneously.

The wavelength emitted is a function of the band-gap of the semiconductor and the modes of the optical cavity. In general, the maximum gain will occur for photons with energy slightly above the band-gap energy, and the modes nearest the gain peak will lase most strongly. If the diode is driven strongly enough, additional *side modes* may also lase. Some laser diodes, such as most visible lasers, operate at a single wavelength, but that wavelength is unstable and changes due to fluctuations in current or temperature.

Due to diffraction, the beam diverges (expands) rapidly after leaving the chip, typically at 30 degrees vertically by 10 degrees laterally. A lens must be used in order to form a collimated beam like that produced by a laser pointer. If a circular beam is required, cylindrical lenses and other optics are used. For single spatial mode lasers, using symmetrical lenses, the collimated beam ends up being elliptical in shape, due to the difference in the vertical and lateral divergences. This is easily observable with a red laser pointer.

8. With neat diagram explain the construction and working of LED. (8) (Nov/Dec 2014, Nov/Dec 2012)

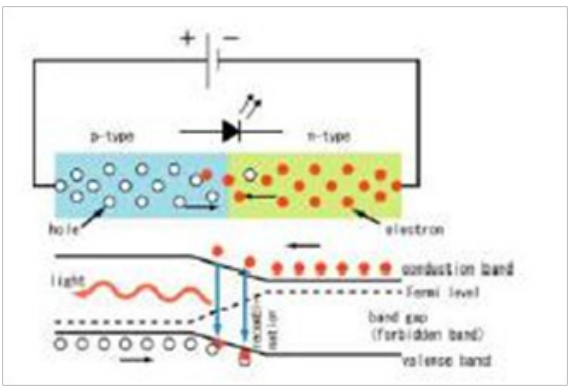
A light-emitting diode (LED) is a semiconductor light source. LEDs are used as indicator lamps in many devices, and are increasingly used for lighting. Introduced as a practical electronic component in 1962, early LEDs emitted low-intensity red light, but modern versions are available

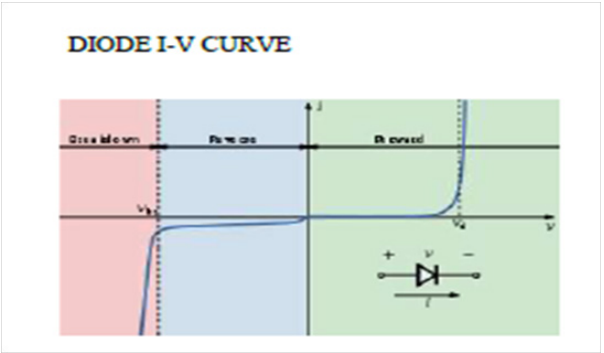
across the visible, ultraviolet and infrared wavelengths, with very high brightness.

When a light-emitting diode is forward biased (switched on), electrons are able to recombine with electron holes within the device, releasing energy in the form of photons. This effect is called electroluminescence and the color of the light (corresponding to the energy of the photon) is determined by the energy gap of the semiconductor. An LED is often small in area

(less than 1 mm2), and integrated optical components may be used to shape its radiation pattern. LEDs present many advantages over incandescent light sources including lower energy consumption, longer lifetime, improved robustness, smaller size, faster switching, and greater durability and reliability. LEDs powerful enough for room lighting are relatively expensive and require more precise current and heat management than compact fluorescent lamp sources of comparable output.

Light-emitting diodes are used in applications as diverse as replacements for aviat ion lighting, automotive lighting (particularly brake lamps, turn signals and indicators) as well as in traffic signals. The compact size, the possibility of narrow bandwidth, switching speed, and extreme reliability of LEDs has allowed new text and video displays and sensors to be developed, while their high switching rates are also useful in advanced communications technology. Infrared LEDs are also used in the remote control units of many commercial products including televisions, DVD players, and other domestic appliances.





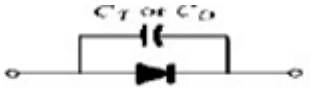
9. Write down the expression for transient capacitance and diffusion capacitance (8) (April/May 2017, Nov/Dec 2016)

Electronic devices are inherently sensitive to very high frequencies. Most shunt capacitive effects that can be ignored at lower frequencies because the reactance XC=1/2πfC is very large (open circuit equivalent). This, however, cannot be ignored at very high frequencies. XC will become sufficiently small due to the high value of f to introduce a low-reactance "shorting" path. In the p-n semiconductor diode, there are two capacitive effects to be considered. In the reverse-bias region we have the transition- or depletion region capacitance (CT), while in the forward-bias region we have the diffusion (CD) or storage capacitance.

Recall that the basic equation for the capacitance of a parallel plate capacitor is defined by C=€A/d, where € is the permittivity of the dielectric (insulator) between the plates of area A separated by a distance d. In the reverse-, bias region there is a depletion region (free of carriers) that behaves essentially like an insulator between the layers of opposite charge. Since the depletion width (d) will increase with increased reverse-bias potential, the resulting transition capacitance will decrease.

The fact that the capacitance is dependent on the applied reverse-bias potential has application in a number of electronic systems. Although the effect described above will also be present in the forward-bias region, it is over shadowed by a capacitance effect directly dependent on the rate at which charge is injected into the regions just outside the depletion region.

The capacitive effects described above are represented by a capacitor in parallel with the ideal diode, as shown in the figure. For low- or mid-frequency applications (except in the power area), however, the capacitor is normally not included in the diode symbol.



Including the effect of the transition or diffusion capacitance on the semiconductor diode

Diode capacitances: The diode exhibits two types of capacitances transition capacitance and diffusion capacitance.

- Transition capacitance: The capacitance which appears between positive ion layer in n-region and negative ion layer in p-region.
- Diffusion capacitance: This capacitance originates due to diffusion of charge carriers in the opposite regions.

The transition capacitance is very small as compared to the diffusion capacitance.

In reverse bias transition, the capacitance is the dominant and is given by:

$$C_T = C A / W$$

where CT - transition capacitance

A - diode cross sectional area

W - depletion region width

In forward bias, the diffusion capacitance is the dominant and is given by:

$$C_D = dQ / dv = \tau^* dI / dV = \tau^* g = \tau / r\,(\text{general})$$

where CD - diffusion capacitance

dQ - change in charge stored in depletion region

V - change in applied voltage

- time interval for change in voltage

g - diode conductance

r - diode resistance

The diffusion capacitance at low frequencies is given by the formula:

$$C_D = \tau^* g / 2\,(\text{low frequency})$$

The diffusion capacitance at high frequencies is inversely proportional to the frequency and is given by the formula:

$$C_D = g(\tau / 2\omega)^{1/2}$$

Note: The variation of diffusion capacitance with applied voltage is used in the design of varactor.

10. Explain the break down mechanisms i) Avalanche and ii) Zener breakdown in detail. (Nov/Dec2015)

When an ordinary P-N junction diode is reverse biased, normally only very small reverse saturation current flows. This current is due to movement of minority carriers. It is almost independent of the voltage applied. However, if the reverse bias is increased, a point is reached when the junction breaks down and the reverse current increases abruptly. This current could be large enough to destroy the junction. If the reverse current is limited by means of a suitable series resistor, the power dissipation at the junction will not be excessive, and the device may be operated continuously in its breakdown region to its normal (reverse saturation) level. It is found that for a suitably designed diode, the breakdown voltage is very stable over a wide range of reverse currents. This quality gives the breakdown diode many useful applications as a voltage reference source.

The critical value of the voltage, at which the breakdown of a P-N junction diode occurs, is called the *breakdown voltage.* The breakdown voltage depends on the width of the depletion region, which, in turn, depends on the doping level. The junction offers almost zero resistance at the breakdown point.

There are two mechanisms by which breakdown can occur at a reverse biased P-N junction:

1. Avalanche breakdown and
2. Zener breakdown.

Avalanche breakdown

The minority carriers, under reverse biased conditions, flowing through the junction acquire a kinetic energy which increases with the increase in reverse voltage. At a sufficiently high reverse

voltage (say 5 V or more), the kinetic energy of minority carriers becomes so large that they knock out electrons from the covalent bonds of the semiconductor material. As a result of collision, the liberated electrons in turn liberate more electrons and the current becomes very large leading

to the breakdown of the crystal structure itself. This phenomenon is called the avalanche breakdown. The breakdown region is the knee of the characteristic curve. Now the current is not controlled by the junction voltage but rather by the external circuit.

Zener breakdown

Under a very high reverse voltage, the depletion region expands and the potential barrier increases leading to a very high electric field across the junction. The electric field will break some of the covalent bonds of the semiconductor atoms leading to a large number of free minority carriers, which suddenly increase the reverse current. This is called the Zener effect. The breakdown occurs at a particular and constant value of reverse voltage called the breakdown voltage, it is found that Zener breakdown occurs at electric field intensity of about 3 x 107 V/m.

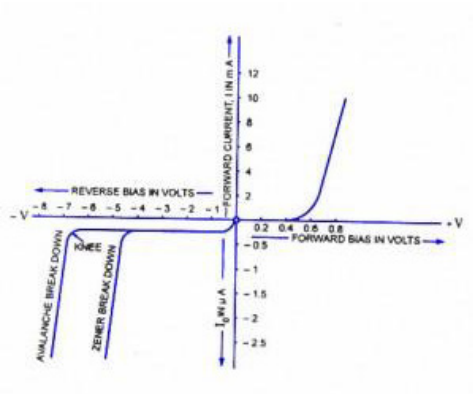


Fig 1.18: Diode characteristics with breakdown

Either of the two (Zener breakdown or avalanche breakdown) may occur independently, or both of these may occur simultaneously. Diode junctions that breakdown below 5 V are caused by

Zener effect. Junctions that experience breakdown above 5 V are caused by avalanche effect. Junctions that breakdown around 5 V are usually caused by combination of two effects. The Zener breakdown occurs in heavily doped junctions (P-type semiconductor moderately doped and N-type heavily doped), which produce narrow depletion layers. The avalanche breakdown occurs in lightly doped junctions, which produce wide depletion layers. With the increase in junction temperature Zener breakdown voltage is reduced while the avalanche breakdown voltage

increases. The Zener diodes have a negative temperature coefficient while avalanche diodes have a positive temperature coefficient. Diodes that have breakdown voltages around 5 V have zero temperature coefficient. The breakdown phenomenon is reversible and harmless so long as the safe operating temperature is maintained.

11. With neat diagram explain the construction and working of Photodiode. (8)

The photo diode is a semiconductor p-n junction device whose region of operation is limited to the reverse biased region. The figure below shows the symbol of photodiode

Fig 1.26:Symbol of photodiode.

Principle of operation:

A photodiode is a type of photo detector capable of converting light into either current or voltage, depending upon the mode of operation. The common, traditional solar cell used to generate electric solar power is a large area photodiode. A photodiode is designed to operate in reverse bias. The deletion region width is large. Under normal conditions it carries small reverse current due to minority charge carriers. When light is incident through glass window on the p-n junction, photons in the light bombard the p-n junction and some energy s imparted to the valence electrons. So valence electrons break covalent bonds and become free electrons. Thus more electron-hole pairs are generated. Thus total number of minority charge carriers increases and hence reverse current increases. This is the basic principle of operation of photo diode.

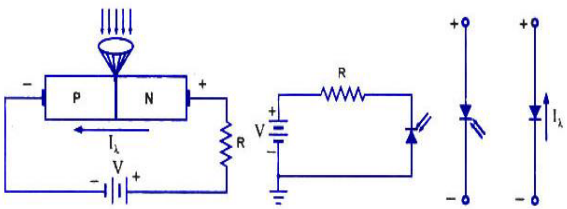


Fig 1.27: Basic Biasing Arrangement and construction of photodiode and symbols

Characteristics of photodiode:

When the P-N junction is reverse-biased, a reverse saturation current flows due to thermally generated holes and electrons being swept across the junction as the minority carriers. With the increase in temperature of the junction more and more hole-electron pairs are created and so the reverse saturation current I0 increases. The same effect can be had by illuminating the junction. When light energy bombards a P-N junction, it dislodges valence electrons. The more light striking the junction the larger the reverse current in a diode. It is due to generation of more and more charge carriers with the increase in level of illumination. This is clearly shown in ' figure for different intensity levels. The dark current is the current that exists when no light is incident. It is to be noted here that current becomes zero only with a positive applied bias equals to VQ. The almost equal spacing between the curves for the same increment in luminous flux reveals that the reverse saturation current I0 increases linearly with the luminous flux as shown in figure. Increase in reverse voltage does not increase the reverse current significantly, because all available charge carriers are already being swept across the junction. For reducing the reverse saturation current I0 to zero, it is necessary to forward bias the junction by an amount equal to barrier potential. Thus the photodiode can be used as a photoconductive device.

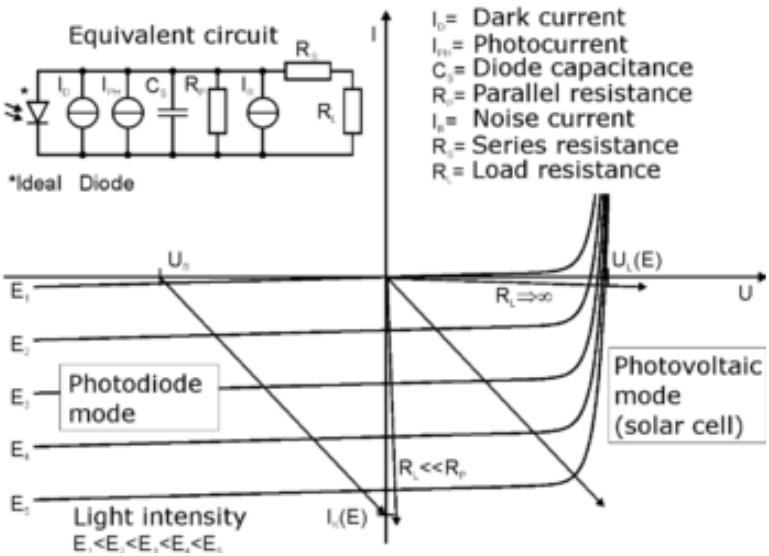


Fig 1.28: characteristics of photodiode

On removal of reverse bias applied across the photodiode, minority charge carriers continue to be swept across the junction while the diode is illuminated. This has the effect of increasing the concentration of holes in the P-side and that of electrons in the N-side But the barrier potential is negative on the P-side and positive on the N-side, and was created by holes flowing from P to N-side and electrons from N to P-side during fabrication of junction. Thus the flow of minority carriers tends to reduce the barrier potential. When an external circuit is connected across the diode terminals, the minority carrier; return to the original side via the external circuit. The electrons which crossed the junction from P to N-side now flow out through the N-terminal and into the P-terminal This means that the device is behaving as a voltage cell with the N-side being the negative terminal and the P-side the positive terminal. Thus, the photodiode is & photovoltaic device as well as photoconductive device.

Advantages:

The advantages of photodiode are:

1.It can be used as variable resistance device.

2.Highly sensitive to the light.

3.The speed of operation is very high.

Disadvantages:

1.Temperature dependent dark current.

2.poor temperature stability.

3.Current needs amplification for driving other circuits.

Applications:

1.Alarm system.

2.counting system.

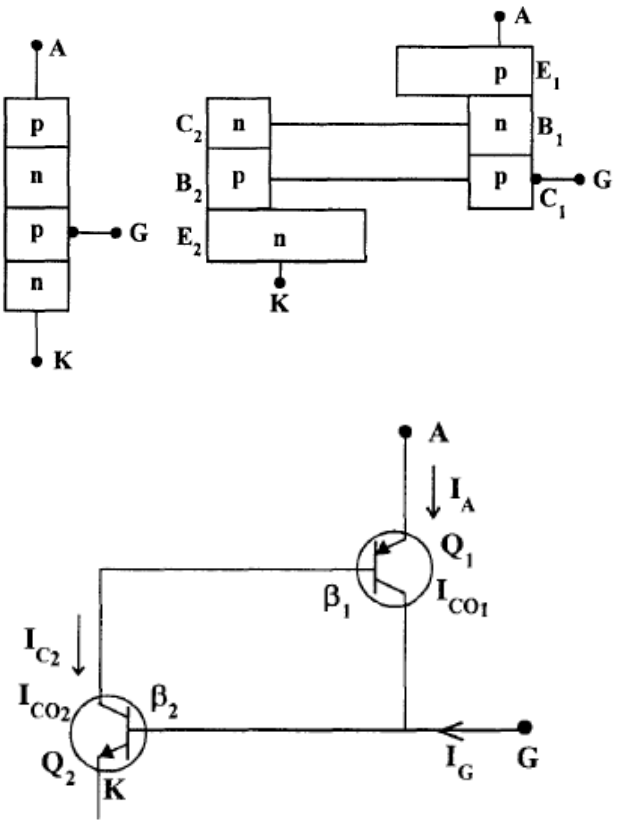
UNIT-II

TRANSISTORS

PART - B

1. Draw the two transistor equivalent circuit of SCR.

(April/May 2017)



Two transistor equivalent circuit of SCR

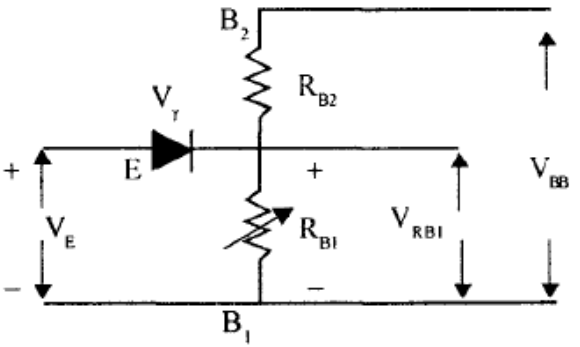
2. A transistor has a typical β of 100. If the collector current is 40 mA, what is the value of emitter current? **(April/May 2017)**

$I_E = I_C + I_B$ and

$I_B = 0.4$ mA

$I_E = 40$ mA + 0.4 mA = **40.4 mA**

3. Define an Intrinsic stand off ratio of UJT and draw its equivalent circuit. (April/May 2017)



Equivalent circuit of UJT

The Intrinsic Stand off Ratio (η) is defined as

Η = Intrinsic Stand off Ratio =

$$= \frac{R_{B1}}{R_{B1} + R_{B2}} \Big| I_E = 0$$

$$= \frac{R_{B1}}{R_{BB}} \Big| I_E = 0$$

Where R_{BB} = Interbase resistance = R_{B1}+R_{B2}

The typical range of η is from 0.5 to 0.8.

4. Compare the performance of CE and CC configuration. (April/May 2017)

Property	CE	CC
Input resistance	Moderate (about 750 Ω)	High(about 750 Ω)
Output resistance	Moderate (about 45 Ω)	Low (about 25 Ω)
Current gain	High	High
Voltage gain	About 500	Less than 1
Phase shift Between input & output voltages	180°	0 or 360°
Applications	For audio frequency circuits	For impedance matching

5. Name the different configurations of BJT. (Nov/Dec 2014)

CB, CE and CC configurations

6. Among CE,CB and CC configurations, which one is the popular? Why? (Nov/Dec 2012)

The CE configuration is widely used because it provides both voltage gain as well as current gain greater than unity.

7. Define cutoff voltage of a transistor.

Cutoff is the lowest voltage at which the transistor operates (linear or saturation)

8. What is a FET?

A field effect transistor is a three terminal semiconductor device in which current conduction is by one type of carriers (either electrons or holes) and is controlled by an electric field.

9. Which device is called as unipolar device? Why?

Since the operation of FET depends upon the flow of majority carriers (either the electrons or holes) only, the FET is said to be unipolar device.

10. What are the main drawbacks in BJT?

The main two drawbacks in BJT are .Low input impedance, Considerable noise level.

11. What is pinch off voltage?

Drain source voltage above which the drain current become constant is known as pinch off voltage. The point N is called as pinch off point. Above the pinch off voltage the channel width becomes narrow and drain current remains constant.

12. What are advantages of FET?

- It is a voltage control, constant current driven device that is the variation in input voltage controls the output current.
- The input impedance is very high so it allows a high degree of isolation between the input and the output circuit.
- The carriers are not crossing the junction hence the noise is highly reduced.

- It has a negative temperature co-efficient of resistance. This can avoid thermal runaway.

13. Define transconductance?

It is the ratio of change in drain current to the change in gate source voltage at constant drain source voltage.

14. Define amplification factor?

It is the product of drain resistance and transconductance

15. State the two types of MOSFET. State also the modes in which they operate.

Types: (a) N- channel MOSFET, (b) P-channel MOSFET

Depletion mode: In this mode the gate is maintained at positive potential with respect to source.

Enhancement mode: In this mode both the gate and drain are maintained at positive potential with respect to source.

16. Why the input impedance of FET is more than that of a BJT?

The input impedance of FET is more than that of BJT because the input circuit of FET is reverse biased whereas the input circuit of BJT is forward biased.

17. What is MOSFET?

The MOSFET is an abbreviation for Metal Oxide Semiconductor Field Effect Transistor. It is a three terminal semiconductor device similar to FET with gate insulated from the channel.

18. What does UJT stands for? Justify the name UJT.

A **unijunction transistor** (**UJT**) is a three-lead electronic semiconductor device with only one junction that acts exclusively as an electrically controlled switch.The UJT is not used as a linear amplifier. It is used in free-running oscillators, synchronized or triggered oscillators, and pulse generation circuits at low to moderate frequencies (hundreds of kilohertz). It is widely used in the triggering circuits for silicon controlled rectifiers.

19. Differentiate BJT and FET. (April/May 2015)

FET	BJT
1. It is a unipolar device	It is a biopolar device
2.It is a voltage controlled device	It is a current driven device
3.Its input resistance is very high.	Its input resistance is very low
4. It is less noisy.	It is comparatively more noisy.
5. No thermal runaway	There is thermal runaway
6. High switching speed	Lower switching speed.

20. Difference between MOSFET and FET

FET	MOSFET
It is operated only in depletion mode	The depletion MOSFET can be operated in both depletion mode and enhancement mode.
High drain resistance	Higher drain resistance.

21. Difference between UJT and BJT?

UJT	BJT
1. It has only one PN junction	It has two PN junctions
2. The three terminals are labeled as Emitter(E), Base1 (B_1) and Base2 (B_2)	The three terminals are labeled as Emitter (E), Base (B) and Collector(C).
3.It has no ability to amplify signals	It can amplify signals.

22. What is meant by negative resistance region of UJT?

In a UJT when the emitter voltage reaches the peak point voltage (V_p), emitter current starts flowing. After the peak point any effort to increase in emitter voltage (V_E) further leads to sudden increase in the emitter current with corresponding decrease in V_E, exhibiting negative resistance. This takes place until the valley point is reached. The region between the peak point and valley point is called “negative resistance region”.

23. Name the special features of a FET?

High input resistance , Low noise,Better thermal stability, High power gain, High frequency response.

24. Define voltage variable resistance ?

FET can also be used in the region before pinch off. FET can also be used as a voltage control resistor. For this operation the drain to source resistance is controlled by the voltage V_{GS}. Hence it is called as voltage variable resistor V_{BR}.

25. The noise level in FET is very small. Why?

In FET, for current conduction no junction is involved. The conduction is either through an N- type or P-type semiconductor. Therefore, the noise level is very small.

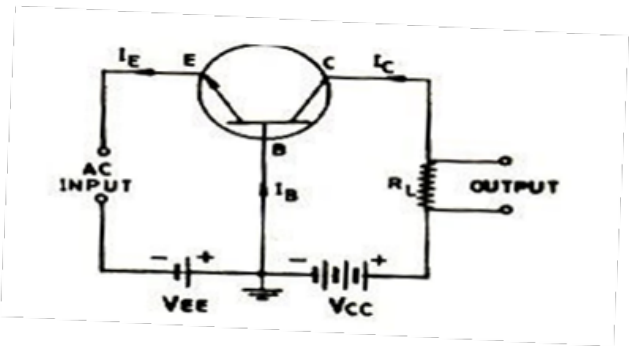
26. Power MOSFET is a voltage controlled device. Why?

Power MOSFET is voltage controlled device because its output characteristics are determined by the field which depends on Voltage applied.

27. Calculate β of a transistor when α = 0.98.

$\beta = \alpha/1-\alpha = 0.98/1-0.98 = 49$

28. Draw the circuit of NPN transistor in CB configuration?



29. What are power transistors? List it's applications.

Power transistors are designed for power amplification which means that the operating voltage and\ must be large.

Applications:

1. They are used in switching power supplies.

2. They are used in audio power amplifiers.

30. What is the relation between IB,IE and IC in CB configuration?

Emitter current $I_E=I_B+I_C$

31. Name the operating modes of a transistor?

1.Cut off

2.Active

3.Saturation

32. When does a transistor acts as a switch?

The transistor acts as a switch when it is operated at either cutoff region or saturation region.

PART-B

1. Explain in detail about structure, operation, characteristics and biasing of BJT. (NOV/DEC2014)

The transistor formed by back to back connection of two diodes.

Bipolar Junction Transistors : The operation of the transistor depends on both majority and minority carriers.

The voltage between two terminals controls the current through the third terminal. So it is called current controlled device.

It can be use as amplifier and logic switches. BJT consists of three terminal:

- collector : C
- base : B
- emitter : E

Two types of BJT : pnp and npn

Transistor Construction

3 layer semiconductor device consisting:

- 2 n- and 1 p-type layers of material - npn transistor
- 2 p- and 1 n-type layers of material - pnp transistor

The term bipolar reflects the fact that holes and electrons participate in the injection process into the oppositely polarized material

A single pn junction has two different types of bias:

- forward bias
- reverse bias

Thus, a two-pn-junction device has four types of bias.

Position of the terminals and symbol of BJT.

Base is located at the middle and more thin from the level of collector and emitter

The emitter and collector terminals are made of the same type of semiconductor material, while the base of the other type of material

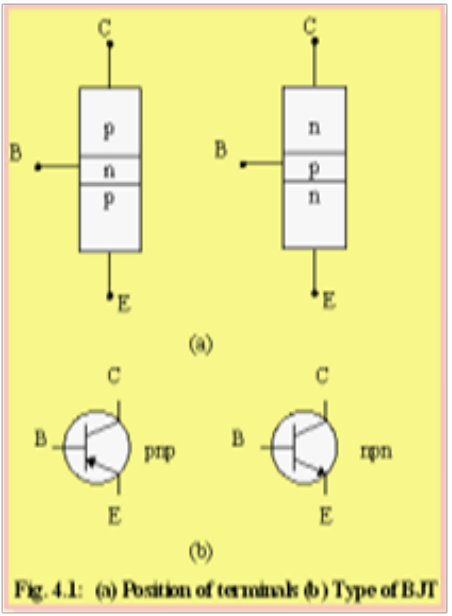
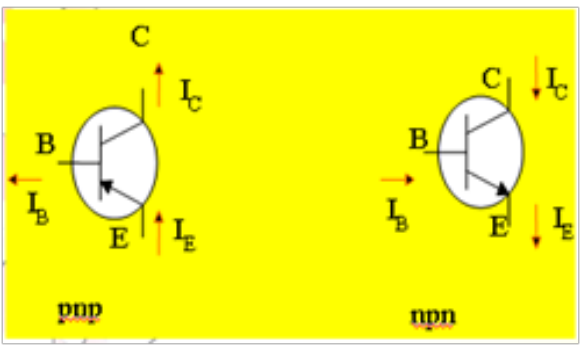


Fig. 4.1: (a) Position of terminals (b) Type of BJT

Transistor currents



The arrow is always drawn on the emitter The arrow always point toward the n-type

The arrow indicates the direction of the emitter current:

pnp:E-> B

npn: B-> E

IC = the collector current

IB = the base current

IE = the emitter current

Transistor Operation

The basic operation will be described using the pnp transistor. The operation of the pnp transistor is exactly the same if the roles played by the electron and hole are interchanged.

One p-n junction of a transistor is reverse-biased, whereas the other is forward-biased

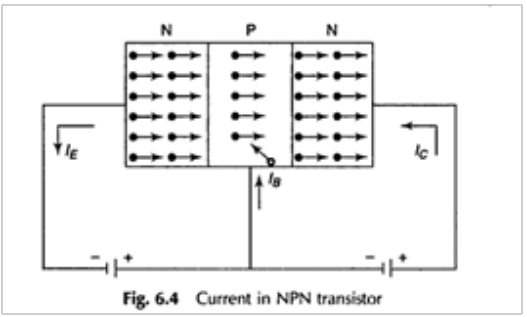


Fig. 6.4 Current in NPN transistor

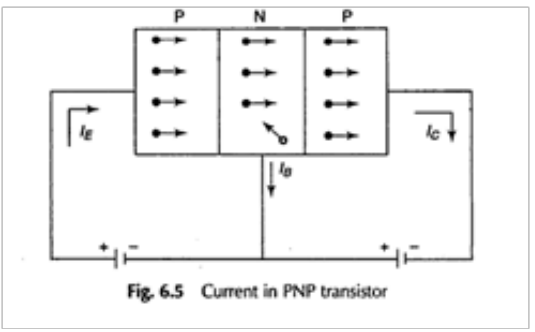


Fig. 6.5 Current in PNP transistor

Both biasing potentials have been applied to a pnp transistor and resulting majority and minority carrier flows indicated.

Majority carriers (+) will diffuse across the forward-biased p-n junction into the n-type material.

A very small number of carriers (+) will through n-type material to the base terminal. Resulting IB is typically in order of microamperes.

The large number of majority carriers will diffuse across the reverse-biased junction into the p-type material connected to the collector terminal.

Majority carriers can cross the reverse-biased junction because the injected majority carriers will appear as minority carriers in the n-type material.

Applying KCL to the transistor :

$$I_E = I_C + I_B$$

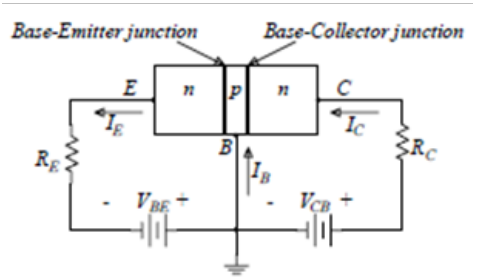
The comprises of two components – the majority and minority carriers

$$I_C = I_{Cmajority} + I_{COminority}$$

$I_{CO} – I_C$ current with emitter terminal open and is called leakage current.

CURRENT EUATIONS

let‘s consider the BJT npn structure shown on Figure.



With the voltage V_{BE} and V_{CB} as shown, the Base-Emitter (B-E) junction is forward biased and the Base Collector (B-C) junction is reverse biased.

The current through the B-E junction is related to the B-E voltage as

$$I_E = I_s\left(e^{V_m(V_r)} - 1\right)$$

Due to the large differences in the doping concentrations of the emitter and the base regions the electrons injected into the base region (from the emitter region) results in the emitter current I_E.

Furthermore the number of electrons injected into the collector region is directly related to the electrons injected into the base region from the emitter region.

Therefore, the collector current is related to the emitter current which is in turn a function of the B-E voltage.

The collector current and the base current are related by

$$I_c = \beta I_B$$

And by applying KCL we obtain

$$I_E = I_c + I_B$$

And thus from equations the relationship between the emitter and the base currents is

$$I_E = (1+\beta)I_B$$

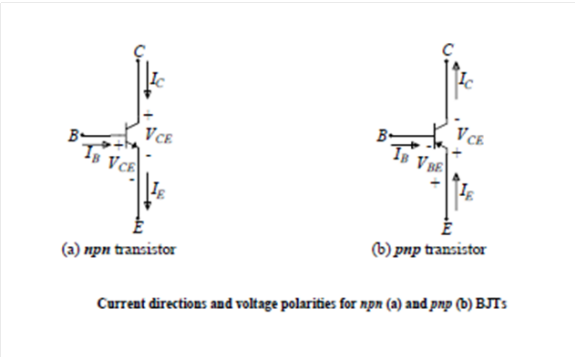
And equivalently

$$I_c = (\beta / 1+\beta) I_E$$

The fraction (β / 1+β) is called α,

For the transistors of interest β=100 which corresponds to α= 0.99 and $I_c = I_B$

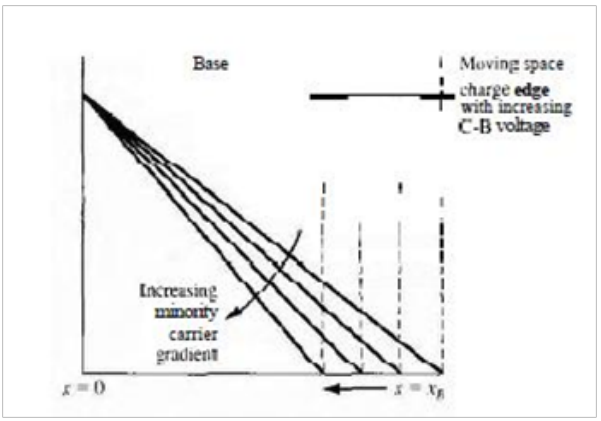
The direction of the currents and the voltage polarities for the npn and the pnp BJTs are shown in fig.



Current directions and voltage polarities for *npn* (a) and *pnp* (b) BJTs

Early Voltage (Base width modulation)

As the voltages applied to the base-emitter and base-collector junctions are changed, the depletion layer widths and the quasi-neutral regions vary as well. This causes the collector current to vary with the collector-emitter voltage as illustrated in Figure .



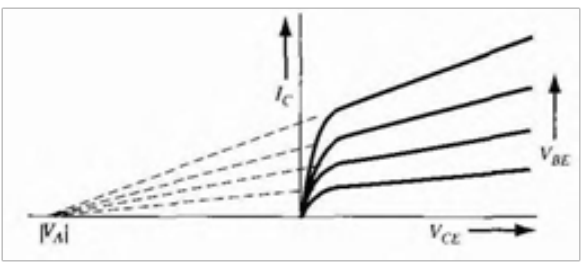
Variation of the minority-carrier distribution in the base quasi-neutral region due to a variation of the base-collector voltage.

A variation of the base-collector voltage results in a variation of the quasi-neutral width in the base. The gradient of the minority-carrier density in

the base therefore changes, yielding an increased collector current as the collector-base current is increased. This effect is referred to as the Early effect. The Early effect is observed as an increase in the collector current with increasing collector-emitter voltage as illustrated with Figure. The Early voltage, VA, is obtained by drawing a line tangential to the transistor I-V characteristic at the point of interest. The Early voltage equals the horizontal distance between the point chosen on the I-V characteristics and the intersection between the tangential line and the horizontal axis. It is indicated on the figure by the horizontal arrow.

The change of the collector current when changing the collector-emitter voltage is primarily due to the variation of the base-collector voltage, since the base-emitter junction is forward biased and a constant base current is applied. The collector current depends on the base-collector voltage since the base-collector depletion layer width varies, which also causes the quasi-neutral width, wB , in the base to vary. This variation can be calculated for a piece-wise uniformly-doped transistor using the ideal transistor mode.

$$\frac{C}{CE} \cong -\frac{dI_C}{dV_{BC}} = \frac{I_C}{w'_B}\frac{dw'_B}{dV_{BC}} \qquad (1)$$



Collector current increase with an increase of the collector-emitter voltage due to the Early effect. The Early voltage, V_A, is also indicated on the figure.

This variation can be expressed by the Early voltage, VA, which quantifies what voltage variation would result in zero collector current.

$$\frac{dI_C}{dV_{CE}} = \Delta\frac{I_C}{[V_A]} \qquad (2)$$

It can be shown that the Early voltage also equals the majority carrier charge in the base, QB, divided by

the base-collector junction capacitance, *Cj,BC = εs/(xp,BC+xn,BC)*

where *xp,BC* and *xn,BC* are given

by (6) .

$$[V_A] = \frac{Q_p, B}{C_j, BC} = \frac{qN_B w'_B}{\frac{\delta_S}{x_p, BC + x_n, BC}} \qquad .....(3)$$

The Early voltage can also be linked to the output conductance, *r0*, which equals:

$$r_0 = \Delta \frac{dV_{CE}}{dI_C} = \frac{|V_A|}{I_C} \qquad .....(4)$$

In addition to the Early effect, there is a less pronounced effect due to the variation of the base-emitter voltage,

which changes the ideality factor of the collector current. However, the effect at the base-emitter junction is

much smaller since the base-emitter junction capacitance is larger and the base-emitter voltage variation is very limited since the junction is forward biased. This effect does lead to a variation of the ideality factor, *n*, given by,

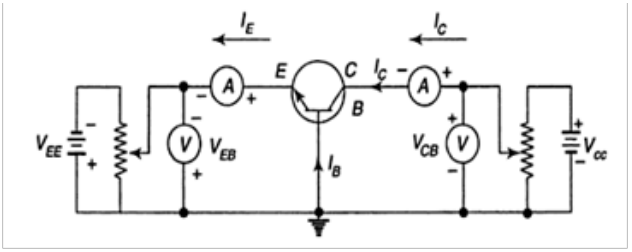
$$n = \frac{1}{V_t \frac{d \ln I_C}{dV_{BE}}} \cong 1 + \frac{V_t}{Q_{p,B}} C_{j,BE} = 1 + \frac{V_t C_{j,BE}}{[V_A] C_{j,BC}}$$

$$I_C = I_{C,s} \left[\exp\left(\frac{V_{BE}}{nV_t} \right) - 1 \right]$$

Where the $I_{c,s}$ is the collector saturation current.

2. Explain the input and output characteristics of a CB configuration using NPN BJT. (Nov/Dec 2016, May/June 2014)

In common base configuration circuit is shown in figure. Here base is grounded and it is used as the common terminal for both input and output. It is also called as grounded base configuration. Emitter is used as a input terminal where as collector is the output terminal.



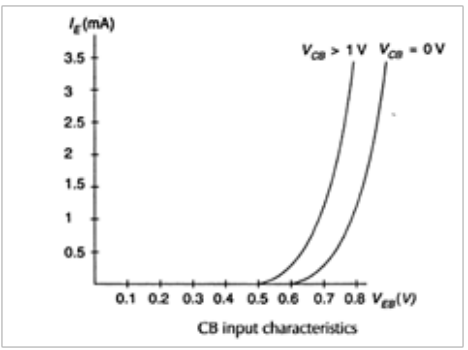
Input Characteristics

It is defined as the characteristic curve drawn between input voltage to input current whereas output voltage is constant.

To determine input characteristics, the collector base voltage V_{CB} is kept constant at zero and emitter current IE is increased from zero by increasing V_{EB}.

This is repeated for higher fixed values of V_{CB}.

A curve is drawn between emitter current and emitter base voltage at constant collector base voltage is shown in figure.



When V_{CB} is zero EB junction is forward biased. So it behaves as a diode so that emitter current increases rapidly.

Output Characteristics

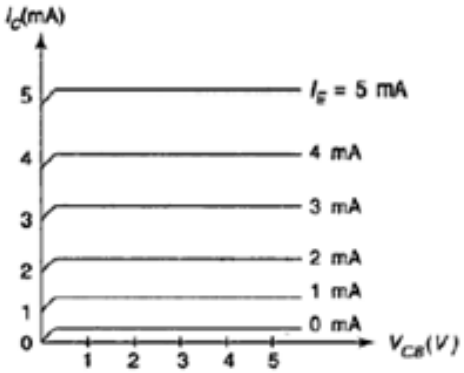
It is defined as the characteristic curve drawn between output voltage to output current whereas input current is constant.

To determine output characteristics, the emitter current I_E is kept constant at zero and collector current I_c is increased from zero by increasing V_{CB}.

This is repeated for higher fixed values of I_E.

From the characteristic it is seen that for a constant value of I_E, I_c is independent of V_{CB} and the curves are parallel to the axis of V_{CB}.

As the emitter base junction is forward biased the majority carriers that is electrons from the emitter region are injected into the base region.



CB output characteristics

In CB configuration a variation of the base-collector voltage results in a variation of the quasi- neutral width in the base. The gradient of the minority-carrier density in the base therefore changes, yielding an increased collector current as the collector-base current is increased. This effect is referred to as the Early effect.

Transistor parameters in CB configuration

The slope of CB characteristics will give the following four transistor parameters. It is known as base hybrid parameters.

I.Input impedance (h_{ib}): It is defined as the ratio of change in input voltage (emitter voltage) to change in input current (emitter current) with the output voltage (collector voltage) is kept constant.

$$h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E}, V_{CB}\ \text{constant}$$

This ranges from 20ohms to 50ohms.

II.Output admittance (h_{ob}): It is defined as the ratio of change in output current (collector current) to change in output voltage (collector voltage) with the input current (emitter current) is kept constant.

$$h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}}, I_E\ \text{constant}$$

This ranges from 0.1 to 10μ mhos.

III.Forward current gain (h_{fb}): It is defined as the ratio of change in output current (collector current) to change in input current (emitter current) with the output voltage (collector voltage) is kept constant.

$$h_{fb} = \frac{\Delta I_C}{\Delta I_E}, V_{CB} \text{ constant}$$

This ranges from 0.9 to 1.0.

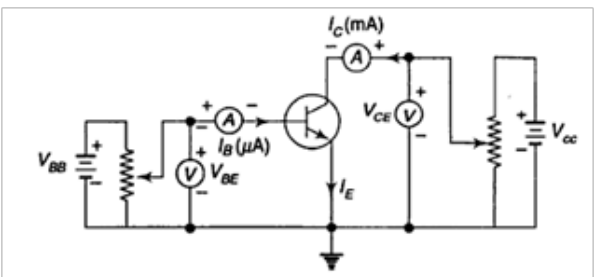
IV.Reverse voltage gain (h_{rb}): It is defined as the ratio of change in input voltage (emitter voltage) to change in output voltage (collector voltage) with the input current (emitter current) is kept constant.

$$h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}}, I_E \text{ constant}$$

This ranges from 10-5 to 10-4.

3. Explain the input and output characteristics of a CE configuration using NPN BJT. (Nov/Dec 2013)

In common emitter configuration circuit is shown in figure. Here emitter is grounded and it is used as the common terminal for both input and output. It is also called as grounded emitter configuration. Base is used as a input terminal whereas collector is the output terminal.



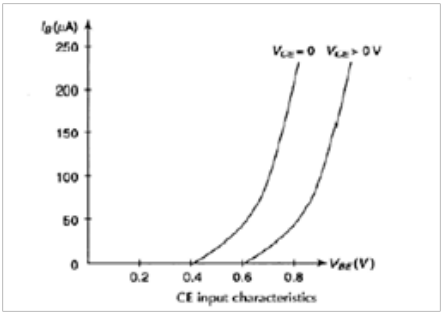
Input Characteristics

It is defined as the characteristic curve drawn between input voltage to input current whereas output voltage is constant.

To determine input characteristics, the collector base voltage V_{CB} is kept constant at zero and base current I_B is increased from zero by increasing V_{BE}.

This is repeated for higher fixed values of V_{CE}.

A curve is drawn between base current and base emitter voltage at constant collector base voltage is shown in figure.



Here the base width decreases. So curve moves right as V_{CE} increases.

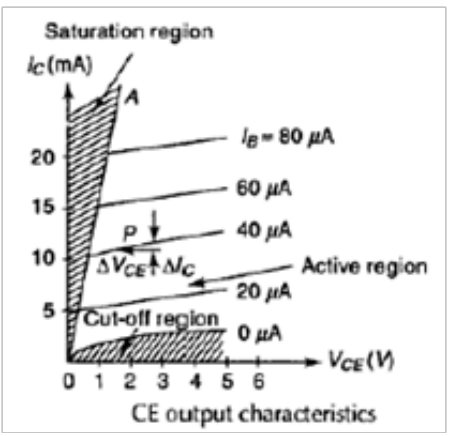
Output Characteristics

It is defined as the characteristic curve drawn between output voltage to output current whereas input current is constant.

To determine output characteristics, the base current I_B is kept constant at zero and collector current I_C is increased from zero by increasing V_{CE}.

This is repeated for higher fixed values of I_B..

From the characteristic it is seen that for a constant value of I_B, I_C is independent of V_{CB} and the curves are parallel to the axis of V_{CE}.



The output characteristic has 3 basic regions:

- Active region –defined by the biasing arrangements
- Cutoff region – region where the collector current is 0A
- Saturation region- region of the characteristics to the left of V_{CB} = 0V

Active region	Saturation region	Cut-off region
I_E increased, I_C increased BE junction forward bias and CB junction reverse bias. Refer to the graf, $I_C \approx I_E$ I_C not depends on V_{CB} Suitable region for the transistor working as amplifier	BE and CE junction is forward bias Small changes in V_{CB} will cause big different to I_C The allocation for this region is to the left of $V_{CB} = 0V$.	Region below the line of $I_E = 0A$ BE and CB is reverse bias No current flow at collector, only leakage current

Transistor parameters in CE configuration

The slope of CE characteristics will give the following four transistor parameters. It is known as emitter hybrid parameters.

I.Input impedance (h_{ie}): It is defined as the ratio of change in input voltage (base voltage) to change in input current (base current) with the output voltage (collector voltage) is kept constant.

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B}.V_{CE}\,\text{constant}$$

This ranges from 500ohms to 2000ohms.

II.Output admittance (h_{oe}): It is defined as the ratio of change in output current (collector current) to change in output voltage (collector voltage) with the input current (base current) is kept constant.

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}.I_B\,\text{constant}$$

This ranges from 0.1 to 10μ mhos.

III.Forward current gain (h_{fe}): It is defined as the ratio of change in output current (collector current) to change in input current (base current) with the output voltage (collector voltage) is kept constant.

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B}.V_{CE}\,\text{constant}$$

This ranges from 20 to 200.

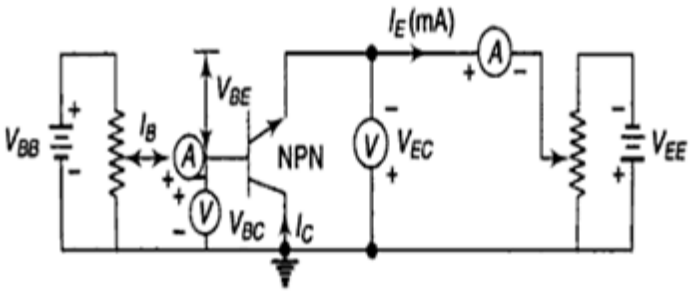
IV. Reverse voltage gain (h_{re}): It is defined as the ratio of change in input voltage (base voltage) to change in output voltage (collector voltage) with the input current (base current) is kept constant.

$$e = \frac{\Delta V_{BE}}{\Delta V_{CE}}, I_B \text{ constant}$$

This ranges from 10^{-5} to 10^{-4}.

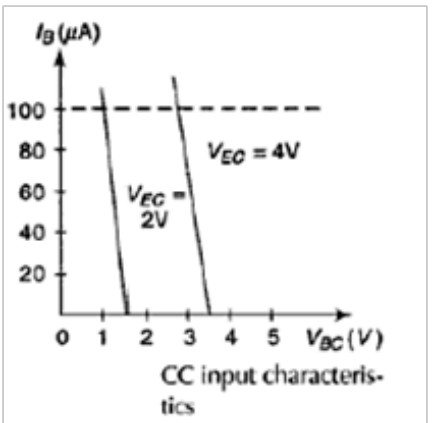
4. Explain the input and output characteristics of a CC configuration using NPN BJT.

In common collector configuration circuit is shown in figure. Here collector is grounded and it is used as the common terminal for both input and output. It is also called as grounded collector configuration. Base is used as a input terminal whereas emitter is the output terminal.



Input Characteristics

It is defined as the characteristic curve drawn between input voltage to input current whereas output voltage is constant.



To determine input characteristics, the emitter base voltage V_{EB} is kept constant at zero and base current I_B is increased from zero by increasing V_{BC}.

This is repeated for higher fixed values of V_{CE}.

A curve is drawn between base current and base emitter voltage at constant collector base

voltage is shown in above figure.

Output Characteristics

It is defined as the characteristic curve drawn between output voltage to output current whereas

input current is constant.

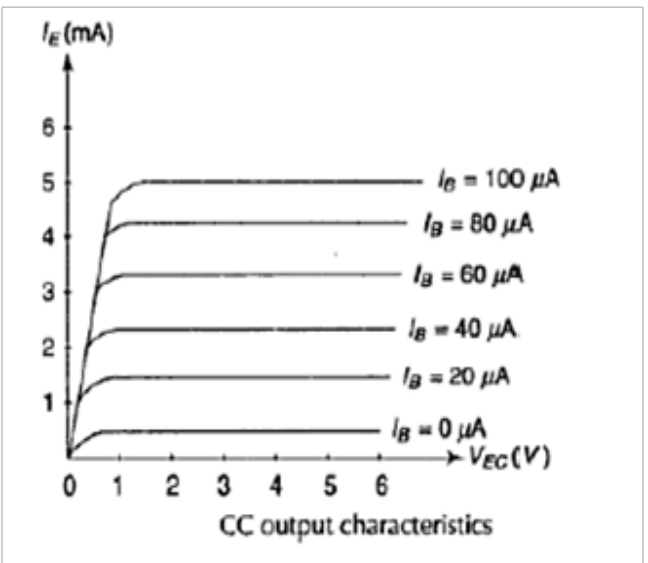
To determine output characteristics, the base current I_B is kept constant at zero and emitter

current I_E is increased from zero by increasing V_{EC}.

This is repeated for higher fixed values of I_B.

From the characteristic it is seen that for a constant value of I_B, I_E is independent of V_{EB} and the

curves are parallel to the axis of V_{EC}.



Transistor parameters in CC configuration

The slope of CC characteristics will give the following four transistor parameters. It is known as base hybrid parameters.

I.Input impedance (h_{ic}): It is defined as the ratio of change in input voltage (base voltage) to change in input current (base current) with the output voltage (emitter voltage) is kept constant.

$$h_{ic} = \frac{\Delta V_{ac}}{\Delta I_B}.V_{EC}\ \text{cons tan t}$$

II.Output admittance (h_{oc}): It is defined as the ratio of change in output current (emitter current) to change in output voltage (emitter voltage) with the input current (base current) is kept constant.

$$h_{oc} = \frac{\Delta I_E}{\Delta V_{EG}}.I_B\ \text{cons tan t}$$

III.Forward current gain ($h_{fc)}$: It is defined as the ratio of change in output current (emitter current) to change in input current (base current) with the output voltage (emitter voltage) is kept constant.

$$h_{fc} = \frac{\Delta I_E}{\Delta I_B}.V_{EG}\text{cons tan t}$$

IV. Reverse voltage gain (h_{rc}): It is defined as the ratio of change in input voltage (base voltage) to change in output voltage (emitter voltage) with the input current (base current) is kept constant.

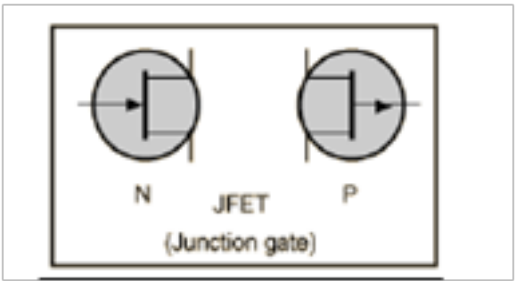
$$h_{rc} = \frac{\Delta V_{ac}}{\Delta V_{EG}}, I_B\text{cons tan t}$$

A comparison of CB, CE and CC Configurations

Property	CB	CE	CC
Input resistance	Low (about 100 Ω)	Moderate (about 750 Ω)	High(about 750 Ω)
Output resistance	High (about 450 Ω)	Moderate (about 45 Ω)	Low (about 25 Ω)
Current gain	1	High	High
Voltage gain	About 150	About 500	Less than 1

Phase shift Between input ?& output voltages	0 or 360°	180°	0 or 360°
Applications	For high frequency circuits	For audio frequency circuits	For impedance matching

5. Explain in detail about structure, operation, characteristics and biasing of JFET. (April/May 2017, Nov/Dec 2016)

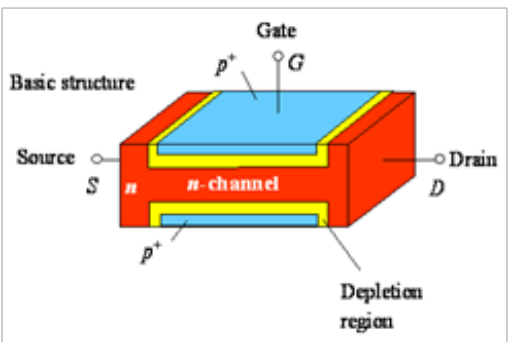


JFETs consists of a piece of high-resistivity semiconductor material (usually Si) which constitutes a channel for the majority carrier flow.

Conducting semiconductor channel between two ohmic contacts – source & drain. JFET is a high-input resistance device, while the BJT is comparatively low.

If the channel is doped with a donor impurity, n-type material is formed and the channel current will consist of electrons.

If the channel is doped with an acceptor impurity, p-type material will be formed and the channel current will consist of holes.



N-channel devices have greater conductivity than p-channel types, since electrons have higher mobility than do holes; thus n-channel JFETs are approximately twice as efficient conductors compared to their p-channel counterparts.

The magnitude of this current is controlled by a voltage applied to a gate, which is a reverse- biased.

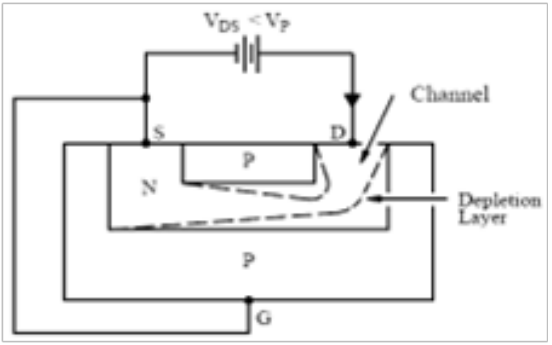
The fundamental difference between JFET and BJT devices: when the JFET junction is reverse- biased the gate current

is practically zero, whereas the base current of the BJT is always some value greater than zero.

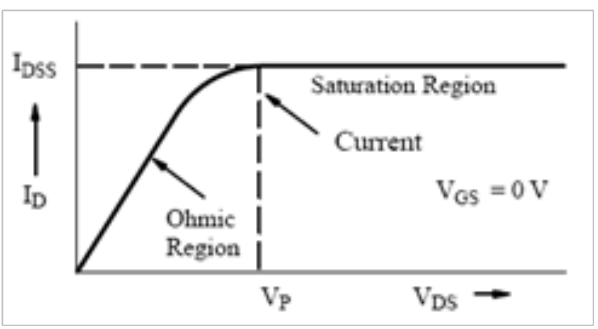
Basic structure of JFETs

In addition to the channel, a JFET contains two ohmic contacts: the source and the drain.

- The JFET will conduct current equally well in either direction and the source and drain leads are usually interchangeable. N-channel JFET
- This transistor is made by forming a channel of N-type material in a P-type substrate.
- Three wires are then connected to the device.
- One at each end of the channel.
- One connected to the substrate.
- In a sense, the device is a bit like a PN-junction diode, except that there are two wires connected to the N-type side
- The gate is connected to the source.
- Since the pn junction is reverse-biased, little current will flow in the gate connection.
- The potential gradient established will form a depletion layer, where almost all the electrons present in the n-type channel will be swept away. The most depleted portion is in the high field between the G and the D, and the least-depleted area is between the G and the S.

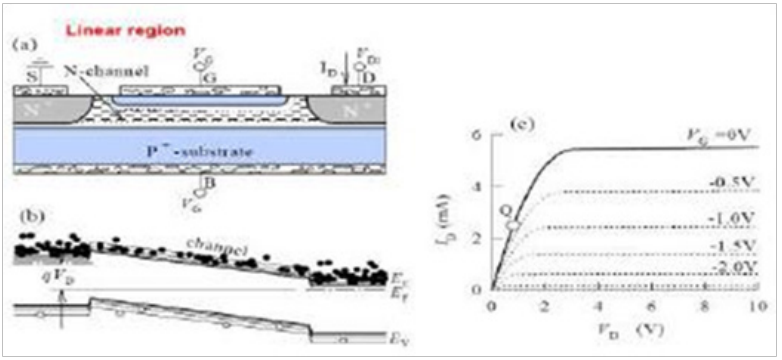


- Because the flow of current along the channel from the (+ve) drain to the (-ve) source is really a flow of free electrons from S to D in the n-type Si, the magnitude of this current will fall as more Si becomes depleted of free electrons.
- There is a limit to the drain current (I_D) which increased V_{DS} can drive through the channel.
- This limiting current is known as I_{DSS} (Drain-to-Source current with the gate shorted to the source).
- The output characteristics of an n-channel JFET with the gate short-circuited to the source.
- The initial rise in I_D is related to the buildup of the depletion layer as V_{DS} increases.
- The curve approaches the level of the limiting current I_{DSS} when I_D begins to be pinched off.
- The physical meaning of this term leads to one definition of pinch-off voltage, V_P , which is the value of V_{DS} at which the maximum I_{DSS} flows.



- With a steady gate-source voltage of 1 V there is always 1 V across the wall of the channel at the source end.
- A drain-source voltage of 1 V means that there will be 2 V across the wall at the drain end. (The drain is ‗up' 1V from the source potential and the gate is 1V ‗down', hence the total difference is 2V.)
- The higher voltage difference at the drain end means that the electron channel is squeezed down a bit more at this end.
- When the drain-source voltage is increased to 10V the voltage across the channel walls at the drain end increases to 11V, but remains just 1V at the source end.
- The field across the walls near the drain end is now a lot larger than at the source end.
- As a result the channel near the drain is squeezed down quite a lot.
- Increasing the source-drain voltage to 20V squeezes down this end of the channel still more.
- As we increase this voltage we increase the electric field which drives electrons along the open part of the channel.
- However, also squeezes down the channel near the drain end.
- This reduction in the open channel width makes it harder for electrons to pass.
- As a result the drain-source current tends to remain constant when we increase the drain source voltage.
- Increasing V_{DS} increases the widths of depletion layers, which penetrate more into channel and hence result in more channel narrowing toward the drain.
- The resistance of the n-channel, R_{AB} therefore increases with V_{DS}.
- The drain current: $I_{DS} = V_{DS}/R_{AB}$
- I_D versus V_{DS} exhibits a sub linear behavior, see figure for $V_{DS} < 5V$.
- The pinch-off voltage, V_P is the magnitude of reverse bias needed across the p+n junction to make them just touch at the drain end.
- Since actual bias voltage across p+n junction at drain end is V_{GD}, the pinch-off occur whenever: $V_{GD} = -V_P$.

JFET: I-V characteristics



6. Explain the working principle of DEPLETION-TYPE MOSFET with necessary diagrams.

(Nov/Dec 2016, Nov/Dec 2015, Apr/May 2015)

DEPLETION-TYPE MOSFET

MOSFETs are further broken down into depletion type and enhancement type. The terms depletion and enhancement define their basic mode of operation, while the label MOSFET stands for metal-oxide-semiconductor-field-effect transistor.

Basic Construction

The basic construction of the n-channel depletion-type MOSFET is provided in Fig. A slab of p-type material is formed from a silicon base and is referred to as the substrate. It is the foundation upon which the device will be constructed. In some cases the substrate is internally

connected to the source terminal. However, many discrete devices provide an additional terminal labeled SS, resulting in a four-terminal device, such as that appearing in Fig. 1

The source and drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel as shown in the figure. The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin silicon dioxide (SiO2) layer. SiO2 is a particular type of insulator referred to as a dielectric that sets up opposing (as revealed by the prefix di-) electric fields within the dielectric when exposed to an externally applied field.

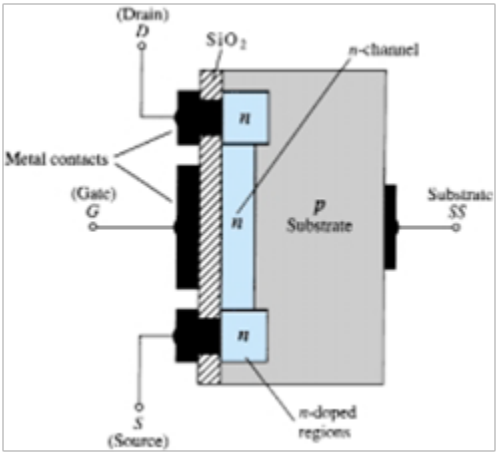


Fig. 1 n – channel depletion type MOSFET

There is no direct electrical connection between the gate terminal and the channel of a MOSFET. It is the insulating layer of SiO2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.

Basic Operation and Characteristics

In Fig. 2 the gate-to-source voltage is set to zero volts by the direct connection from one terminal to the other, and a voltage V_{DS} is applied across the drain-to-source terminals. The result is an attraction for the positive potential at the drain by the free electrons of the n-channel and a current similar to that established through the channel of the JFET. In fact, the resulting current with V_{GS} = 0 V continues to be labeled I_{DSS}, as shown in Fig. 3.

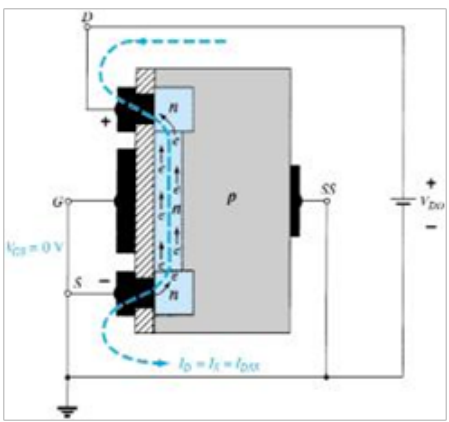


Fig 2. n – channel depletion type MOSFET with V_{GS} = 0 V

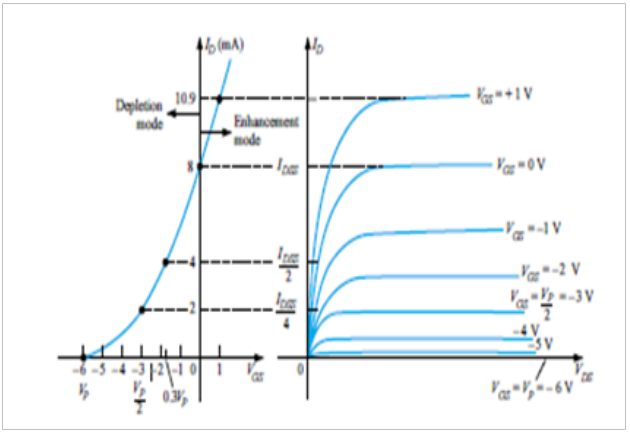


Fig 3. Drain and transfer characteristics

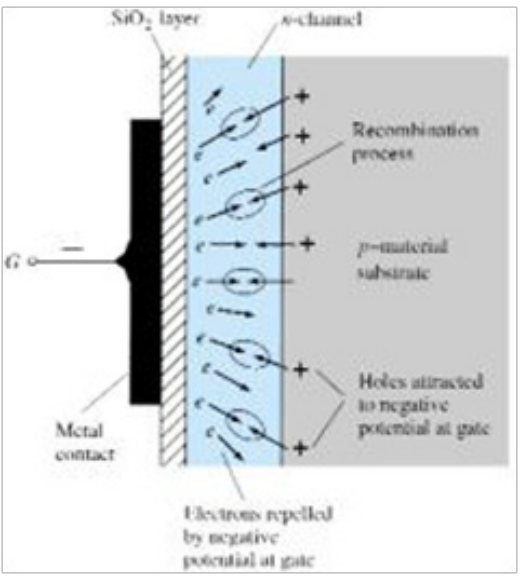


Fig.4 Reduction in free carriers in channel due to –ve potential

In Fig. 4, V_{GS} has been set at a negative voltage such as -1 V. The negative potential at the gate will tend to pressure electrons toward the p-type substrate (like charges repel) and attract holes from the p-type substrate (opposite charges attract) as shown in Fig. 4. Depending on the magnitude of the negative bias established by V_{GS}, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the n-channel available for conduction. The more negative the bias, the higher the rate of recombination.

For positive values of V_{GS}, the positive gate will draw additional electrons (free carriers) from the p-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles. As the gate-to-source voltage continues to increase in the positive direction, Fig. 3 reveals that the drain current will increase at a rapid rate.

7. Explain the working principle of ENHANCEMENT-TYPE MOSFET with necessary diagrams.

(April/May 2017, Nov/Dec 2016, Nov/Dec2015, Apr/May2015)

ENHANCEMENT-TYPE MOSFET Basic Construction

The basic construction of the n-channel enhancement-type MOSFET is provided in Fig.1. A slab of p-type material is formed from a silicon base and is again referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal, while in other cases a fourth lead is made available for external control of its potential level.

The SiO2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the p-type material. In summary, therefore, the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.

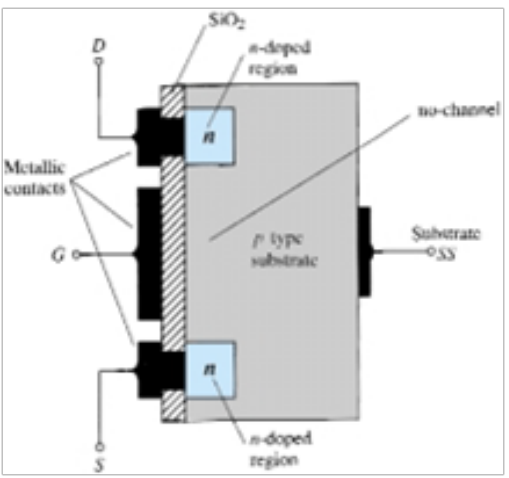


Fig 1. N channel enhancement type MOSFET Basic

Operation and Characteristics

If V_{GS} is set at 0 V and a voltage applied between the drain and source of the device of Fig. 1, the absence of an n-channel (with its generous number of free carriers) will result in a current of effectively zero amperes—quite different from the depletion- type MOSFET and JFET where I_D - I_{DSS}. It is not sufficient to have a large accumulation of carriers (electrons) at the drain and source (due to the n-doped regions) if a path fails to exist between the two. With V_{DS} some positive voltage, V_{GS} at 0 V, and terminal SS directly connected to the source, there are in fact two reverse-biased p-n junctions between the n-doped regions and the p-substrate to oppose any significant flow between drain and source.

In Fig. 2 both V_{DS} and V_{GS} have been set at some positive voltage greater than 0 V, establishing the drain and gate at a positive potential with respect to the source. The positive potential at the gate will pressure the holes (since like charges repel) in the p-substrate along the edge of the SiO_2 layer to leave the area and enter deeper regions of the p-substrate, as shown in the figure.

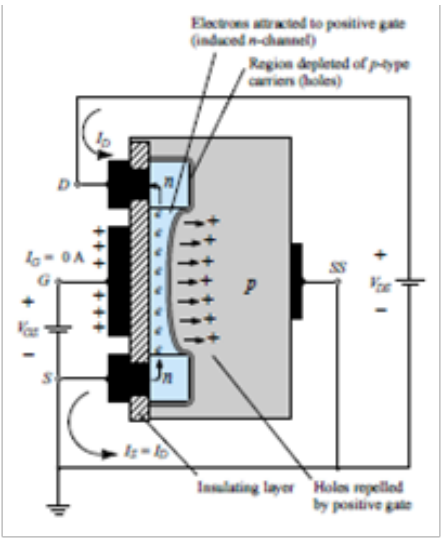


Fig 2. Channel formation

As V_{GS} is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold V_{GS} constant and increase the level of V_{DS}, the drain current will eventually reach a saturation level as occurred for the JFET and depletion-type MOSFET. The leveling off of I_D is due

to a pinching-off process depicted by the narrower channel at the drain end of the induced channel as shown in Fig. 3. Applying Kirchhoff's voltage law to the terminal voltages of the MOSFET of

we find that

$$V_{DG} = V_{DS} - V_{GS}$$

The drain characteristics of Fig. 5.34 reveal that for the device of Fig 3 with $V_{GS} = 8$ V, saturation occurred at a level of $V_{DS} = 6$ V. In fact, the saturation level for V_{DS} is related to the level of applied V_{GS} by

$$V_{DSsat} = V_{GS} - V_T$$

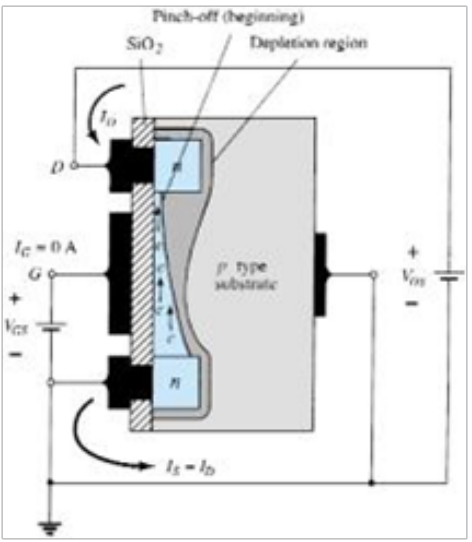


Fig 3. Change in channel and depletion region with increasing V_{DS}

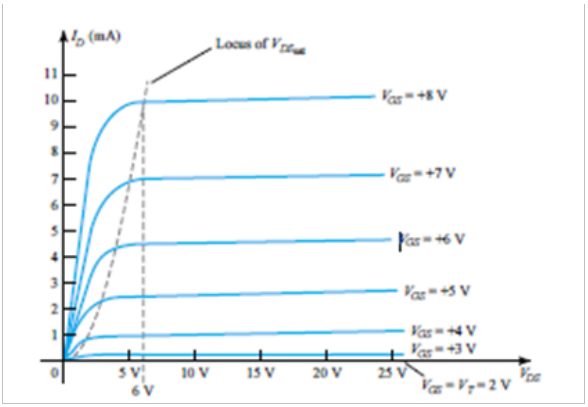


Fig 4. Drain characteristics

For levels of $V_{GS} > V_T$, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$I_D = k(V_{GS} - V_T)^2$$

Again, it is the squared term that results in the nonlinear (curved) relationship between I_D and V_{GS}. The k term is a constant that is a function of the construction of the device. The value of k can be determined from the following equation where $I_{D(on)}$ and $V_{GS(on)}$ are the values for each at a particular point on the characteristics of the device.

$$k = \frac{I_{D(on)}}{\left(V_{as(on)} - V_{\gamma}\right)^2}$$

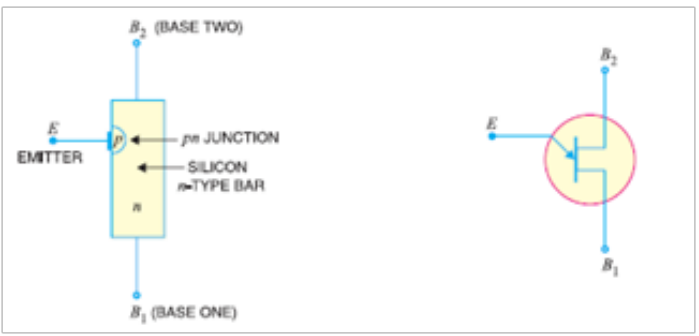
8. Explain structure and characteristics of UJT.

(NOV/DEC2015,APR/MAY2015)

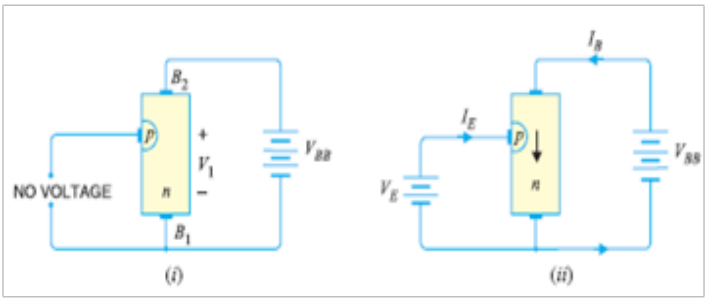
Uni Junction Transistor (UJT)

A unijunction transistor (UJT) is an electronic semiconductor device that has only one junction. The UJT has three terminals: an emitter (E) and two bases (B_1 and B_2).

The base is formed by lightly doped n-type bar of silicon. Two ohmic contacts B_1 and B_2 are attached at its ends. The emitter is of p-type and it is heavily doped. The resistance between B_1 and B_2, when the emitter is open-circuit is called interbase resistance.



Since the device has one pn junction and three leads it is commonly called UJT.**Operation**



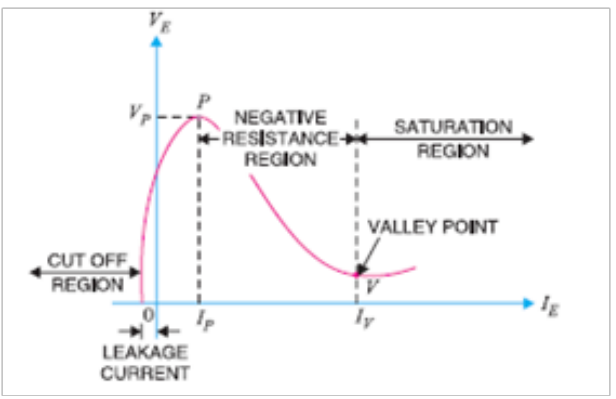
The device has normally B_2 is positive w.r.t B_1.

(i) If voltage V_{BB} is applied between B_2 and B_1 with emitter open (fig. i) a voltage gradient is established along the n type bar. The voltage V_1 between emitter and B_1 establishes a reverse bias of pn junction and the emitter current is cut off. Small leakage current flows from B_2 to emitter.

(ii)If a positive voltage is applied at E (fig. ii) the pn junction remains reverse biased as long as the input is less than V_1. The voltage exceeds V_1 the pn junction become forward biased. Here holes are injected from p type towards B_1. The device is ON state.

(iii) If a negative pulse is applied to E, the pn junction is reverse biased and the emitter current is cut off. The device is OFF state.

Characteristics



Initially in the cut off region, as V_E increases from zero, slight leakage current flows from terminal B_2 to the emitter.

Above a certain value of V_E forward I_E begins to flow, increasing until the peak voltage V_p and current I_p are reached at point P.

After the peak point P an attempt to increase V_E is followed by a sudden increase in emitter current I_E with a corresponding decrease in V_E. This is a negative resistance portion of the curve because in I_E, V_E decreases.

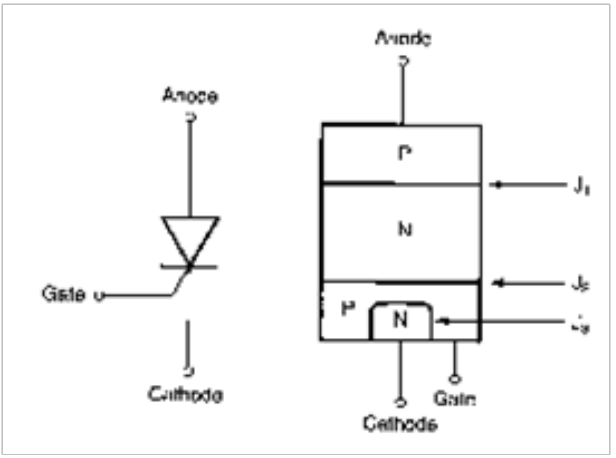
Applications

In switching circuits, Pulse generator and Saw-tooth generator.

9. Explain about SCR.

(APRIL/MAY 2017, NOV/DEC2015, NOV/DEC2014)

Silicon Controlled Rectifier (SCR)



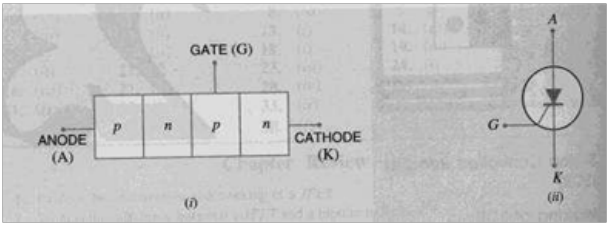
Three terminals

- anode - P-layer
- cathode - N-layer (opposite end)
- gate - P-layer near the cathode

Three junctions - four layers

Connect power such that the anode is positive with respect to the cathode - no current will flow

A silicon controlled rectifier is a semiconductor device that acts as a true electronic switch. It can change alternating current and at the same time can control the amount of power fed to the load. SCR combines the features of a rectifier and a transistor.



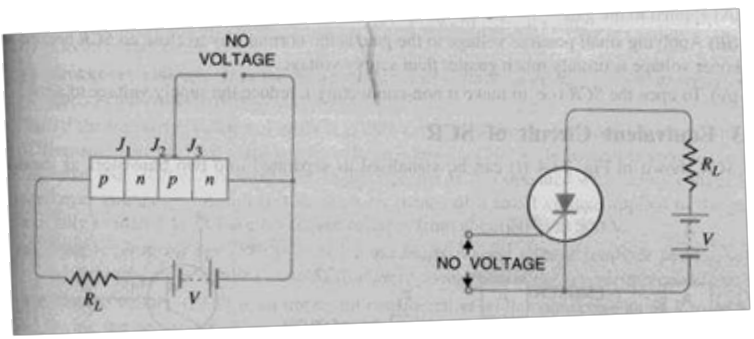
When a pn junction is added to a junction transistor the resulting three pn junction device is called a SCR. ordinary rectifier (pn) and a junction transistor (npn) combined in one unit to form

pnpn device. three terminals are taken : one from the outer p- type material called anode a second from the outer n- type material called cathode K and the third from the base of transistor called Gate. SCR is a solid state equivalent of thyratron. The gate, anode and cathode of SCR correspond to the grid plate and cathode of thyratron SCR is called thyristor.

WORKING PRINCIPLE

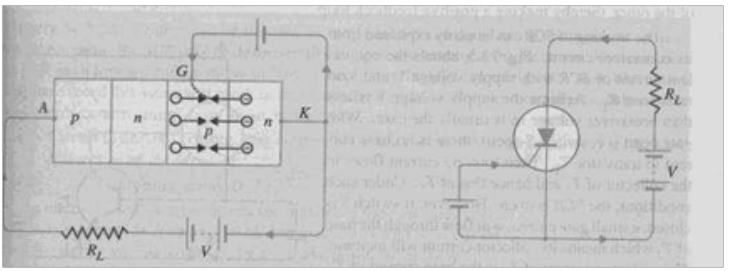
Load is connected in series with anode the anode is always kept at positive potential w.r.t cathode.

WHEN GATE IS OPEN



No voltage applied to the gate, J_2 is reverse biased while J_1 and J_3 are FB . J_1 and J_3 is just in npn transistor with base open no current flows through the load RL and SCR is cut off. If the applied voltage is gradually increased a stage is reached when RB junction J_2 breakdown .the SCR now conducts heavily and is said to be ON state. the applied voltage at which SCR conducts heavily without gate voltage is called Break over Voltage.

WHEN GATE IS POSITIVE W.R.T CATHODE.



The SCR can be made to conduct heavily at smaller applied voltage by applying small positive potential to the gate. J_3 is FB and J_2 is RB the electron from n type material start moving across J_3 towards left holes from p type toward right. Electrons from J_3 are attracted across junction J_2 and gate current starts flowing. as soon as gate current flows anode current increases. the increased anode current in turn makes more electrons available at J_2 breakdown and SCR starts conducting heavily. the gate loses all control if the gate voltage is removed anode current does not decrease at all. The only way to stop conduction is to reduce the applied voltage to zero.

BREAKOVER VOLTAGE

It is the minimum forward voltage gate being open at which SCR starts conducting heavily i.e turned on.

PEAK REVERSE VOLTAGE(PRV)

It is the maximum reverse voltage applied to an SCR without conducting in the reverse direction. HOLDING CURRENT

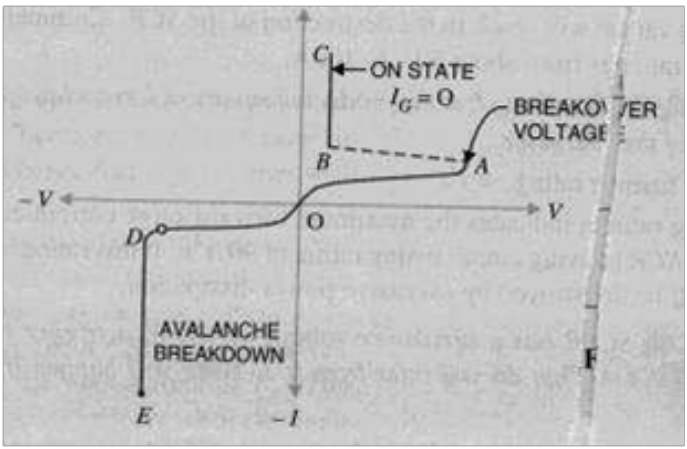
It is the maximum anode current gate being open at which SCR is turned off from on conditions. FORWARD CURRENT RATING

It is the maximum anode current that an SCR is capable of passing without destruction

CIRCUIT FUSING RATING

It is the product of of square of forward surge current and the time of duration of the surge.

VI CHARACTERISTICS OF SCR



FORWARD CHARCTERISTICS

When anode is +ve w.r.t cathode the curve between V & I is called Forward characteristics. OABC is the forward characteristics of the SCR at Ig =0. if the supplied voltage is increased from zero point A is reached . SCR starts conducting voltage across SCR suddenly drops (dotted curve AB) most of supply voltage appears across RL

REVERSE CHARCTERISTICS

When anode is –ve w.r.t.cathode the curve b/w V&I is known as reverse characteristics reverse voltage come across SCR when it is operated with ac supply reverse voltage is increased anode current remains small avalanche breakdown occurs and SCR starts conducting heavily is known as reverse breakdown voltage

Application

- SCR as a switch
- SCR Half and Full wave rectifier
- SCR as a static contactor
- SCR for power control
- SCR for speed control of D.C.Shunt Motor
- Over light detector

10. Explain the structure and characteristics of IGBT.

(April/May 2017)

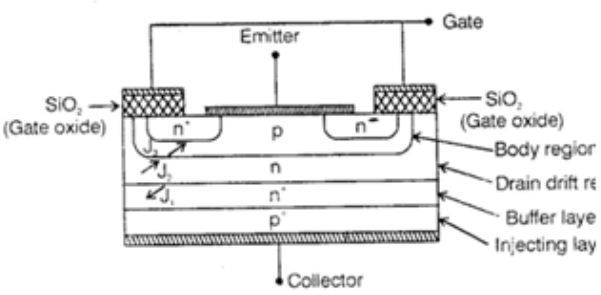
INSULATED GATE BIPOLAR TRANSISTOR (IGBT)

IGBT is a minority-carrier device with high input impedance and large bipolar current carrying capability. It is a device with MOS input characteristics and bipolar output characteristic that is Voltage-controlled bipolar device. It combines the best attributes of both to achieve optimal device characteristic.

IGBT is suitable for many applications in power electronics, especially in pulse width Modulated (PWM) servo and three-phase drives requiring high dynamic range control and low noise. It can also be used in uninterruptible power supplies (UPS) switched-Mode Power supplies (SMPs) requiring high switch repetition rates.

Basic structure

The basic schematic of a N-channel IGBT is shown in the Fig. below



Schematic view of N-channel IGBT

The major difference with the MOSFET cell structure lies in the addition of a p injecting layer. This layer forms a pn junction with the drain layer and injects minority carriers into it The n-type drain layer has two different doping levels. The lightly doped n region is called the drain drift region. The highly doped n+ region is called the buffer layer.

The n- layer at the top is the source or emitter and p layer at the bottom is the drain or collector.

IGBT's without the n' buffer layer, are called non-punch through (NPT) IGBTs whereas those with this layer are called punch-through (PT) IGBTs. The presence of this buffer layer improves the performance of the device

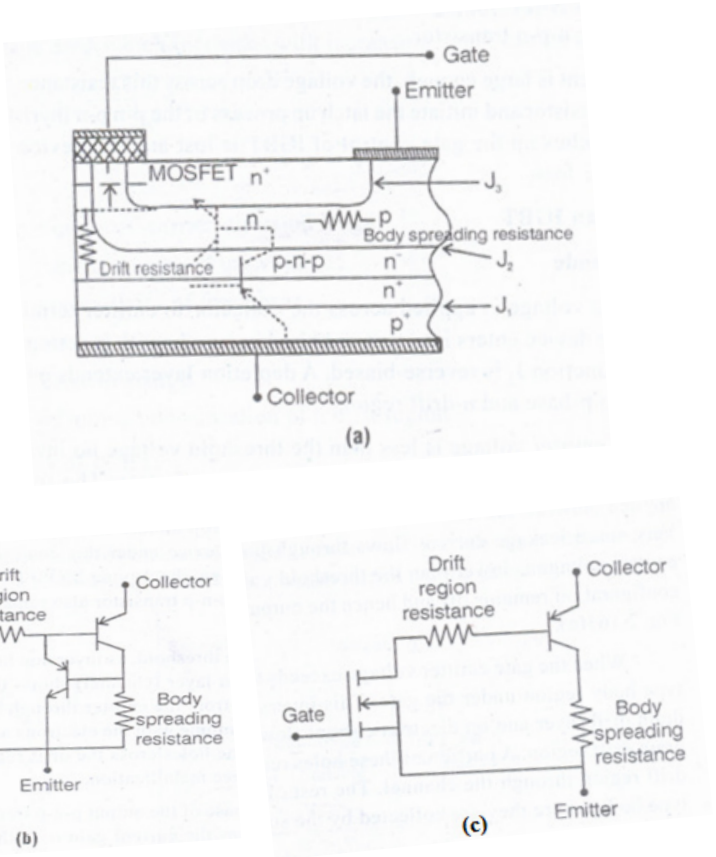
if the doping level and thickness of the layer are chosen appropriately.

The buffer layer performs two main functions:

(i) avoids failure by punch-through action because the depletion region expansion at applied high voltage is restricted by this layer

(ii) (ii) reduces the current during turn off and shortens the fall time of the IGBT because the holes are injected by the p+ collector partially recombine in this layer.

The IGBT cell has a parasitic p-n p-n thyristor structure embedded into it as shown in Fig.



Parasitic thyristor in an IGBT cell (a) Schematic structure (b) Exact equivalent circuit (c) Approximate equivalent circuit

The p-n-p transistor, n-p-n transistor and the driver MOSFET are shown by dotted lines in this figure. Fig.(b) shows the equivalent circuit of the IGBT cell structure. The top p-n-p transistor is formed by p layer as the emitter, the n type drain layer as the base and p injecting layer as the collector.

The lower n-p-n transistor has the n+ type source, the p type body and the n-type drain emitter, base and collector respectively. The base of the lower n-p-n transistor is shorted to the emitter by the emitter metallization. Due to imperfect shorting, the exact equivalent circuit of the IGBT includes the body spreading resistance between the base and the emitter of the lower n-p-n transistor.

If the output current is large enough, the voltage drop across this resistance may forward bias the lower n-p-n transistor and initiate the latch up process of the p-n p-n thyristor structure. Once this structure latches up the gate control of IGBT is lost and the device is destroyed due to excessive power loss.

Operation modes of an IGBT

Forward-Blocking mode

When a positive voltage is applied across the collector-to emitter terminal with gate shorted to emitter, the device enters into forward blocking mode with junctions J_1 and J_3 are forward-biased and junction J_2 is reverse-biased. A depletion layer extends on both sides of junction J_2 partly into p-base and n-drift region

When the gate emitter voltage is less than the threshold voltage no inversion layer is formed in the p-type body region and the device is in the off state. The forward voltage applied between the collector and the emitter drop almost entirely across the junction J_2 Very small leakage current flows through the device under this condition when the gate emitter voltage is lower than the threshold voltage, the driving MOSFET of the Darlington configuration remains off and hence the output p-n-p transistor also remains off as shown in Fig.(C).

When the gate emitter voltage exceeds the threshold, as inversion layer forms in the p type body region under the gate. This inversion layer (channel) shorts the emitter and the drain drift layer and on electron current flows from the emitter through this channel to the drain drift region. A portion of these holes recombine with the electrons arriving at the drain drift region through the channel. The rest of the holes cross the drift region to reach the p type body where they are collected by the source metallization

The n type drain drift region acts as the base of the output p-n-p transistor. The doping level and the thickness of this layer determines the current gain a of the p-n-p transistor. This is kept low so that most of the device current flows through the MOSFET and not the output p-n-p transistor collector. This helps to reduce the voltage drop across the 'body' spreading resistance shown in Fig. (b) and eliminate the possibility of static latch lip of the IGBT

Reversse-Blocking mode:

When a negative voltage is applied across the collector to emitter terminal, the junction becomes reverse – biased and its depletion layer extends into the n drift region. The breakdown voltage during the reverse blocking is determined by an open base BJT formed the p_+ collector / n^- drift/ p-base regions. The device is prone to punch through if the n of region is very lightly dropped. The desired reverse voltage capability is obtained by optimizing the resistivity and thickness of the n^- drift region.

The width of the n drift region that determines the reverse voltage capability and the forward voltage drop which increase with increasing width can be determined by

$$d_1 = \sqrt{\frac{2\varepsilon_o \varepsilon_s V_m}{qN_D}} + L_P$$

Where,

L_P = Minor carrier diffusion length

V_m = maximum blocking voltage

$\varepsilon_{o=}$ Permittivity of free space

ε_1 = dielectric constant of Si

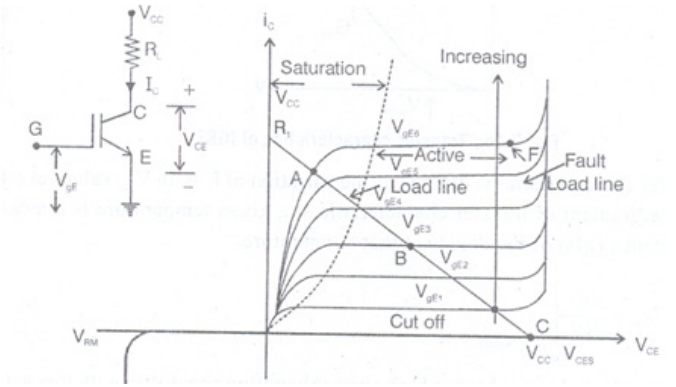
q = electric charge

N_o = Doping concentration of n drift region

Characteristics of IGBT

Input characteristics

The I-V characteristics of an channel IGBT is shown in Fig. 2.164 they appear similar of BJT except that the controlling parameter is not a base current but the gate emitter voltage.



Characteristics of IGBT

It has curves, each of which corresponds to a different gate-to-emitter voltage (V_{CE}). The collector current I_C is measured as a function of collector-emitter voltage (V_{GS}) with the gate-emitter voltage (V_{GE}) constant.

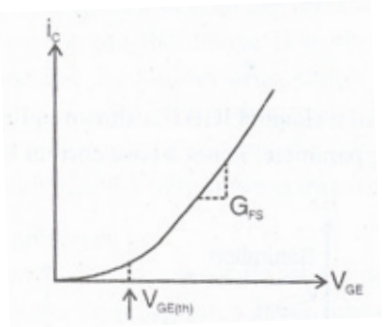
When the gate emitter voltage is below the threshold voltage only a very small leakage current flows through the device while the collector emitter voltage equals the supply voltage (point C in fig. 2) The device, under this condition is said to be operating in the cut-off region.

As the gate emitter voltage increase beyond the threshold voltage the IGBT enters into the active region of operation. In this mode, the collector IC is determined by the transfer characteristics of the device, as is linear over the collector correct range. The rate of IC to [VgE-VgE(th)] is called the forward transconductance (Ifs) of the device.

As the gate emitter voltage is increased further IC also increases and for a given load resistance (RL) VCE decreases. At one point VCE becomes less than VgE-VgE(th). Under this condition the driving MOFSET part of IGBT enters into ohmic region and drives the output p-n-p transistor to saturation under this condition the device is said to be the saturation mode. In the saturation mode the voltage drop across the IGBT remains constant reducing with increasing VgE.

Transfer characteristics

The transfer characteristic is shown in Fig.



Transfer Characteristics of IGBT

The transfer characteristics is defined as the variation of I_C with V_{GE} values at different temperature. The gradient of transfer characteristics at a given temperature is a measure of the transconductance (gfs) of the device at that temperature.

$$g_{fs} = \frac{\partial I_c}{\partial V_{GE}}\Big|_{V_{CE}=\text{Constant}}$$

A large gfs is desirable to obtain a high current handling capability with low gate drive voltage.

As the gate emitter voltage increases beyond the threshold voltage the IGBT enters in the active region of operation. This characteristic is similar to that of a power MOSFET and is linear over most of the collector current range.

Advantages of IGBT over a power MOSFET and a BJT:

(i) It has a very low on-state voltage drop due to conductivity modulation and has superior on-state current density. So smaller chip size is possible and the cost can be reduced.

(ii) Low driving power and a simple drive circuit due to the input MOS gate structure. It can be easily controlled as compared to current controlled devices (thyristor BJT in high voltage and high current applications.

(iii) It has superior current conduction capability compared with the bipolar transistors. It also has excellent forward and reverse blocking capabilities.

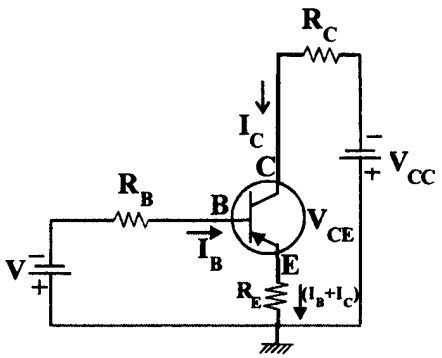
Draw backs:

(1) Switching speed is inferior to that of a power MOSFET and superior to that of a BJT. The collector current failing due to the minority carrier causes the turn-off speed to be slow.

(2) There is a possibility of latch up due to the internal PNPN thyristor structure.

11. Design a circuit with Ge transistor in the self biasing arrangement with V_{CC} = 16V and R_C = 1.5K. The quiescent point is chosen to be V_{CE} = 8V and I_C = 4mA. Stability factor S = 12 is desired β = 50.

Solution:



$$I_B = \frac{I_C}{\beta} = \frac{4}{50} = 80\mu A$$

$$R_e = \frac{V_{CC} - V_{CE} - I_C R_C}{(I_B + I_C)}$$

$$= \frac{16 - 8 - 4 \times 1.5}{4.08} = 0.49k$$

$$s = 12 = \frac{(\beta + 1)1 + \frac{R_B}{R_e}}{1 + \beta + \frac{R_B}{R_e}}$$

$$\frac{R_B}{R_e} = 14.4$$

$$R_B = 14.4 \times R_e = 7.05k$$

V_{BN} = Base to ground voltage

$$= V_{BE} + I_E R_e$$

Therefore, I_E is negative

$$V_{BN} = 0.2 + 4.08 \times 0.49 = 2.2V$$

$$V = V_{BN} + I_B R_b$$

$$= 2.2 + 0.08 \times 7.05 = 2.76V$$

$$V = \frac{R_2 . V_{CC}}{R_1 + R_2}; R_B = \frac{R_1 R_2}{R_1 + R_2}$$

$$\frac{V}{R_B} = \frac{V_{CC}}{R_1} = \frac{16}{R_1}$$

$$\therefore R_1 = \frac{16 R_B}{V}$$

$$= \frac{16 \times 7.05}{2.76} = 41k$$

$$V = 2.76V$$

$$= \frac{R_2 \times V_{CC}}{R_1 + R_2} = \frac{R_2 \times 16}{41k + R_2}$$

$$\therefore R_2 = 8.56k$$

UNIT-III

AMPLIFIERS

PART A

1. What are the two types of small signal model?

The small signal model is of two types

- Low frequency small signal model.
- High frequency small signal model.

2. What are hybrid parameters?

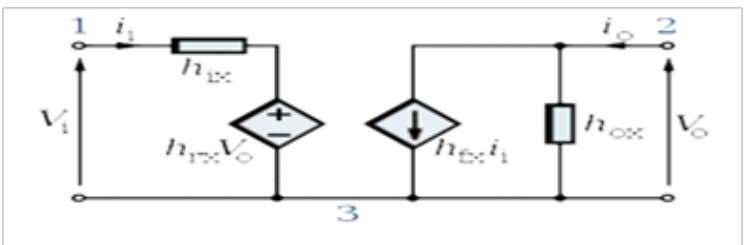
$$h_{11} = \frac{V_i}{I_i}\Big|V_0 = 0$$

$$h_{21} = \frac{I_0}{I_i}\Big|V_0 = 0$$

$$h_{12} = \frac{V_i}{V_0}\Big|I_0 = 0$$

$$h_{22} = \frac{I_0}{V_0}\Big|I_i = 0$$

3. Draw the h-parameter equivalent circuit of a CE BJT configuration? (April/May 2015)



4. Give the h_{ie} and hoe equations of BJT.

- $h_{ie} = \Delta V_{BE}/\Delta I_B|V_{CE}$ Constant
- $h_{oe} = \Delta I_c//\Delta V_c|I_B$ Constant

5. Define Transistor.

Transistor consists of two junctions formed by sandwiching either P-type or N-type semiconductor between a pair of opposite types.

6. Write the current amplification factor for a CB transistor.

a = Change in Collector Current at constant V_{CB} / Change in emitter current.

7. Write the formula for input resistance in a CB transistor.

Input resistance = Change in base - emitter voltage / Change in emitter current at constant

V_{CB}.

8. Write the current amplification factor for a CE transistor.

b = Change in Collector Current / Change in base current at constant V_{CE}.

9. Define transistor action.

A transistor consists of 2 coupled PN junctions. The base is a common region to both junctions and makes a coupling between them. Since the base regions are smaller, a significant interaction between junctions will be available. This is called transistor actions.

10. Define delay time.

It is defined as the time required for the current to rise from 0 to 10% of its maximum value.

11. Define rise time.

It is the time required for the current to rise from 0 to 90 percentage of the maximum value.

12. Define turn-on time.

It is the time required for the current to rise from 0 to 90 percentage of the maximum value ton = $t_d + t_r$.

13. Define fall time.

It is the time required for the Collector current to fall from 90 to 10 percentages of I_{cs}.

14. Define Storage time.

It is the time required to fall from 100 to 90 percent of I_{cs}.

15. Define turn-off time.

It is the time required to fall from 100 to 90 percent of I_{cs}. $T_{off}=t_s+t_r$.

16. Define hybrid parameters.

Any linear circuit having input and output terminals can be analysed by four parameters(one measured on ohm, one in mho and two dimensionless) called hybrid or h parameters.

17. Define power transistors.

Power transistors are those which handle a large amount of current and also dissipates large amount of power across collector base junction.

18. Define current amplification factor in CC transistor.

g =Change in emitter current /Change in base current at constant V_{CE}

19. What are the values of input resistance in CB, CE & CC Configuration

CB - Low about 75

CE - Medium about 750

CC - Very high about 750.

20. Which is the most commonly used transistor configuration? Why?

The CE Configuration is most commonly used.

The reasons are

- High Current gain
- High voltage gain
- High power
- Moderate input to output ratio.

PART-B

1. Draw the h-parameter equivalent circuit of transistor amplifier circuit and derive expression for A_i, R_i, A_v and R_o.
(Nov/Dec 2015, Apr/May 2015, Nov/Dec 2014)

Analysis of a Transistor amplifier circuit using h-parameters:

A transistor amplifier can be constructed by connecting an external load and signal source and biasing the transistor properly.

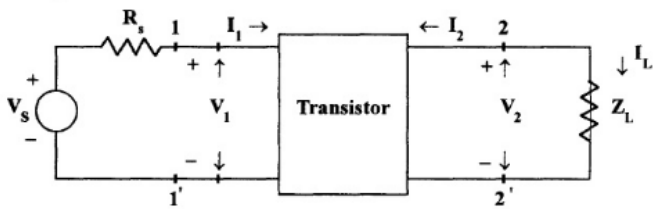


Fig.1.4 Basic Amplifier Circuit

The two port network of Fig. 1.4 represents a transistor in any one of its configuration. It is assumed that h-parameters remain constant over the operating range. The input is sinusoidal and I_1, V_1, I_2 and V_2 are phase quantities

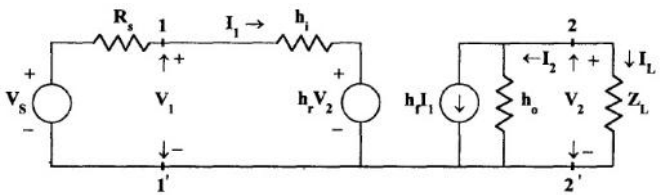


Fig. 1.5 Transistor replaced by its Hybrid Model

Current Gain or Current Amplification (A_i)

For transistor amplifier the current gain A_i is defined as the ratio of output current to input current,i.e,

$$A_i = I_L / I_1 = -I_2 / I_1$$

From the circuit of Fig

$$I_2 = h_f I_1 + h_o V_2$$

Substituting $V_2 = I_L Z_L = -I_2 Z_L$

$$I_2 = h_f I_1 - I_2 Z_L h_o$$

$$I_2 + I_2 Z_L h_o = h_f I_1$$

$$I_2(1+ Z_L h_o) = h_f I_1$$

$$A_i = -I_2 / I_1 = - h_f / (1+ Z_L h_o)$$

Therefore,

$$A_i = - h_f / (1+ Z_L h_o)$$

Input Impedance (Z_i)

In the circuit of Fig , RS is the signal source resistance .The impedance seen when looking into the amplifier terminals (1,1') is the amplifier input impedance Zi,

$$Z_i = V_1 / I_1$$

From the input circuit of Fig $V_1 = h_i I_1 + h_r V_2$

$$Z_i = (h_i I_1 + h_r V_2) / I_1$$

$$= h_i + h_r V_2 / I_1$$

Substituting

$$V_2 = -I_2 Z_L = A_1 I_1 Z_L$$

$$Z_i = h_i + h_r A_1 I_1 Z_L / I_1$$

$$= h_i + h_r A_1 Z_L$$

Substituting for A_i

$$Z_i = h_i - h_f h_r Z_L / (1+ h_o Z_L)$$

$$= h_i - h_f h_r Z_L / Z_L(1/Z_L + h_o)$$

Taking the Load admittance as $Y_L = 1/ Z_L$

$$Z_i = h_i - h_f h_r / (Y_L + h_o)$$

Voltage Gain or Voltage Gain Amplification Factor (A_v)

The ratio of output voltage V_2 to input voltage V_1 give the voltage gain of the transistor i.e,

$$A_v = V_2 / V_1$$

Substituting

$$V_2 = -I_2 Z_L = A_1 I_1 Z_L$$

$$A_v = A_1 I_1 Z_L / V_1 = A_i Z_L / Z_i$$

Output Admittance (Y_o)

Y_o is obtained by setting V_S to zero, Z_L to infinity and by driving the output terminals from a generator V_2. If the current V_2 is I_2 then $Y_o = I_2/V_2$ with $V_S=0$ and RL= ∞.

From the circuit of fig

$$I_2 = h_f I_1 + h_o V_2$$

Dividing by V_2,

$$I_2 / V_2 = h_f I_1/V_2 + h_o$$

With $V_2 = 0$, by KVL in input circuit,

$$R_S I_1 + h_i I_1 + h_r V_2 = 0$$

$$(R_S + h_i) I_1 + h_r V_2 = 0$$

Hence, $I_2 / V_2 = -h_r / (R_S + h_i)$

$$= h_f (-h_r/(R_S + h_i)+h_o$$

$$Y_o = h_o - h_f h_r/(R_S + h_i)$$

The output admittance is a function of source resistance. If the source impedence is resistive then Y_o is real.

Voltage Amplification Factor (A_{vs}) taking into account the resistance (R_s) of the source

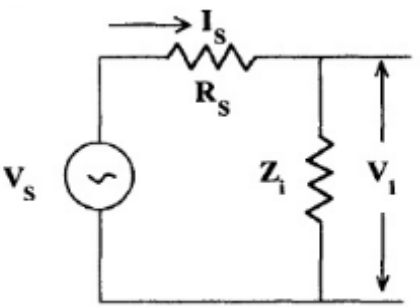


Fig. 5.6 Thevenin's Equivalent Input Circuit

This overall voltage gain A_{vs} is given by

$$A_{vs} = V_2 / V_S = V_2 V_1 / V_1 V_S = A_v V_1 / V_S$$

From the equivalent input circuit using Thevenin's equivalent for the source shown in Fig. 5.6

$$V_1 = V_S Z_i / (Z_i + R_S)$$

$$V_1 / V_S = Z_i / (Z_i + R_S)$$

Then, $A_{vs} = A_v Z_i / (Z_i + R_S)$

Substituting $A_v = A_i Z_L / Z_i$

$$A_{vs} = A_i Z_L / (Z_i + R_S)$$

$$A_{vs} = A_i Z_L R_S / (Z_i + R_S) R_S$$

$$A_{vs} = A_{is} Z_L / R_S$$

Current Amplification (Ais) taking into account the source Resistance (R_S)

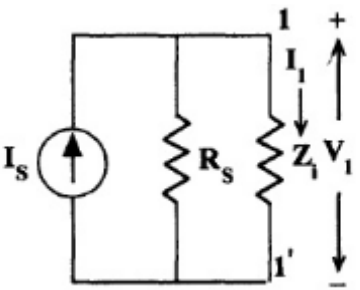


Fig. 1.7 Norton's Equivalent Input Circuit

The modified input circuit using Norton's equivalent circuit for the calculation of A_{is} is shown in Fig. 1.7

Overall Current Gain, $A_{is} = -I_2 / I_S = - I_2 I_1 / I_1 I_S = A_i I_1 / I_S$

From Fig. 1.7 $I_1 = I_S R_S / (R_S + Z_i)$

$$I_1 / I_S = R_S / (R_S + Z_i)$$

and hence, $A_{is} = A_i R_S / (R_S + Z_i)$

Operating Power Gain (A_P)

The operating power gain A_P of the transistor is defined as

$$A_P = P_2 / P_1 = -V_2 I_2 / V_1 I_1 = A_v A_i = A_i A_i Z_L / Z_i$$

$$A_P = A_i^2 \left(\frac{Z_L}{Z_i} \right)$$

Small Signal analysis of a transistor amplifier

$A_i = - h_f / (1+ Z_L h_o)$	$A_v = A_i Z_L / Z_i$
$Z_i = h_i + h_r A_I Z_L$ $= h_i - h_f h_r / (Y_L + h_o)$	$A_{vs} = A_v Z_i / (Z_i + R_S) = A_i Z_L / (Z_i + R_S)$ $= A_{is} Z_L / R_S$
$Y_o = h_o - h_f h_r / (R_S + h_i)$ $= 1/ Z_o$	$A_{is} = A_i R_S / (R_S + Z_i) = A_{vs}$ $= A_{is} Z_L / R_S$

2. Derive the expression for the voltage gain of CS amplifier.
(NOV/DEC2014)

Common Source (CS) Amplifier

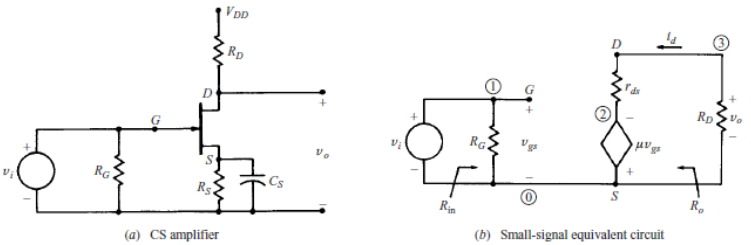


Fig. 5.1 (a) CS Amplifier (b) Small-signal equivalent circuit

A simple Common Source amplifier is shown in Fig. 5.1(a) and associated small signal equivalent circuit using voltage-source model of FET is shown in Fig. 5.1(b)

Voltage Gain

Source resistance (R_S) is used to set the Q-Point but is bypassed by CS for mid-frequency operation.

From the small signal equivalent circuit, the output voltage

$$V_O = -R_D \mu V_{gs} (R_D + r_d)$$

Where $V_{gs} = V_i$, the input voltage,

Hence, the voltage gain,

$$A_V = V_O / V_i = -R_D \mu (R_D + r_d)$$

Input Impedance

From Fig. 5.1(b) Input Impedance is

$$Z_i = R_G$$

For voltage divider bias as in CE Amplifiers of BJT

$$R_G = R_1 \parallel R_2$$

Output Impedance

Output impedance is the impedance measured at the output terminals with the input voltage $V_I = 0$

From the Fig. 5.1(b) when the input voltage $V_i = 0$, $V_{gs} = 0$ and hence $\mu V_{gs} = 0$.

The equivalent circuit for calculating output impedance is given in Fig. 5.2.

Output impedance $Z_o = r_d \parallel R_D$

Normally rd will be far greater than R_D . Hence $Z_o \approx R_D$

3. Discuss the factors involved in the selection of I_c, R_c and R_e for a single stage CE BJT amplifier using voltage divider bias.

The voltage divider as shown in the fig 4.7 is formed using external resistors R_1 and R_2. The voltage across R_2 forward biases the emitter junction. By proper selection of resistors R_1 and R_2, the operating point of the transistor can be made independent of β. In this circuit, the voltage divider holds the base voltage fixed independent of base current provided the divider current is large compared to the base current. However, even with a fixed base voltage, collector current varies with temperature (for example) so an emitter resistor is added to stabilize the Q-point, similar to the above circuits with emitter resistor.

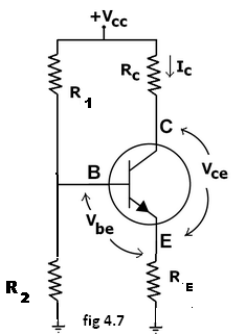


Fig 4.7 Voltage Divider Biasing Circuit

In this circuit the base voltage is given by:

$$V_B = {}_{\text{Voltage across}}\ R_2 = V_{cc}\frac{R_2}{(R_1+R_2)} - I_B\frac{R_1R_2}{(R_1+R_2)}$$

$$\approx V_{cc}\frac{R_2}{(R_1+R_2)}_{\text{Provide}} \qquad I_B << I_2 = V_B / R_2.$$

Also $V_B = V_{be} + I_E R_E$

For the given circuit,

$$I_B = \frac{\frac{V_{cc}}{1+R_1/R_2} - V_{be}}{(\beta+1)R_E + R_1 \,||\, R_2}$$

Let the current in resistor R1 is I1 and this is divided into two parts – current through base and resistor R2. Since the base current is very small so for all practical purpose it is assumed that I1 also flows through R2, so we have

$$I_1 = \frac{V_{cc}}{R_1+R_2}$$

$$V_2 = \frac{V_{CC}}{R_1+R_2}.R_2$$

Applying KVL in the circuit, we have

$$V_2 = V_{BE} + V_E$$

$$V_2 = V_{BE} + I_g R_E$$

$$I_g = \frac{V_2 - V_{BE}}{R_g}$$

$$I_C = \frac{V_2 - V_{BE}}{R_g} \qquad \therefore I_C \cong I_g$$

$$I_C = \frac{\frac{V_{CC}}{R_1+R_2}.R_2 - V_{BE}}{R_E}$$

It is apparent from above expression that the collector current is independent of ? thus the stability is excellent. In all practical cases the value of VBE is quite small in comparison to the V2, so it can be ignored in the above expression so the collector current is almost independent of the transistor

parameters thus this arrangement provides excellent stability. Again applying KVL in collector circuit, we have

$$V_{CC} = I_C R_C + V_{CE} + I_g R_g$$
$$\therefore I_C \cong I_g$$
$$\therefore V_{CC} = I_C R_C + V_{CE} + I_C R_E$$
$$V_{CE} = V_{CC} - I_C \left(R_C + R_g \right)$$

The resistor RE provides stability to the circuit. If the current through the collector rises, the voltage across the resistor RE also rises. This will cause VCE to increase as the voltage V2 is independent of collector current. This decreases the base current, thus collector current increases to its former value.

Stability factor for such circuit arrangement is given by

$$S = \frac{(1+\beta)\left(R_{eq} + R_g\right)}{R_{eq} + R_g (1+\beta)}$$
$$R_{eq} = R_1 \parallel R_2$$
$$S = \frac{(1+\beta)\left(1 + \dfrac{R_{eq}}{R_g}\right)}{\dfrac{R_{eq}}{R_g} + 1 + \beta}$$

If R_{eq}/R_E is very small compared to 1, it can be ignored in the above expression thus we have

$$S = \frac{1+\beta}{1+\beta} = 1$$

Which is excellent since it is the smallest possible value for the stability. In actual practice the value of stability factor is around 8-10, since R_{eq}/R_E cannot be ignored as compared to 1.

Merits:

- Unlike above circuits, only one dc supply is necessary.
- Operating point is almost independent of β variation.
- Operating point stabilized against shift in temperature.

Demerits:

In this circuit, to keep IC independent of β the following condition must be met:

$$I_C = \beta I_B = \beta \frac{\frac{V_{CC}}{1+R_1+R_2} - V_{be}}{(\beta+1)R_E + R_1 \parallel R_2} \approx \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{R_E}$$

$$\text{Which is approximately the case if } (\beta+1)R_E >> R_1 \parallel R_2$$

where $R_1 \parallel R_2$ denotes the equivalent resistance of R_1 and R_2 connected in parallel.

As β-value is fixed for a given transistor, this relation can be satisfied either by keeping R_E fairly large, or making $R_1 \| R_2$ very low.

If R_E is of large value, high V_{CC} is necessary. This increases cost as well as precautions necessary while handling.

If $R_1 \parallel R_2$ is low, either R_1 is low, or R_2 is low, or both are low. A low R_1 raises V_B closer to V_C, reducing the available swing in collector voltage, and limiting how large R_C can be made without driving the transistor out of active mode. A low R_2 lowers V_{be}, reducing the allowed collector current. Lowering both resistor values draws more current from the power supply and lowers the input resistance of the amplifier as seen from the base.

AC as well as DC feedback is caused by R_E, which reduces the AC voltage gain of the amplifier. A method to avoid AC feedback while retaining DC feedback is discussed below.

Usage: The circuit's stability and merits as above make it widely used for linear circuits.

4. Explain the Common Drain MOSFET amplifier and derive its input impedance, output impedance and voltage gain.

(April/May 2017, Nov/Dec 2016)

In this circuit, input is applied between gate and source and output is taken between source and drain.

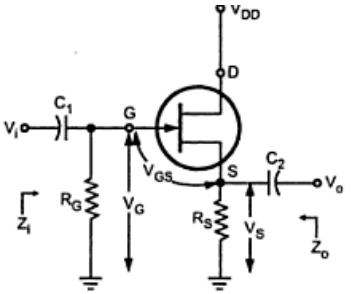


Fig3.12 Circuit of Common Drain amplifier

In this circuit, the source voltage is

$$V_s = V_G + V_{GS}$$

When a signal is applied to the **MOSFET** gate via C_1 ,V_G varies with the signal. As V_{GS} is fairly constant and $V_s = V_G + V_{GS}$, V_s varies with V_i.

The following figure shows the low frequency equivalent model for common drain circuit.

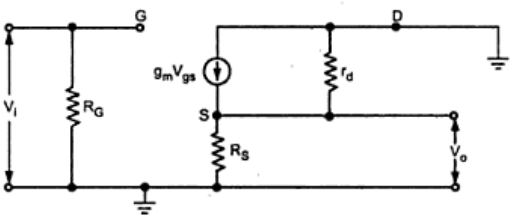


Fig3.13 small model of Common Drain amplifier

Input Impedance Z_i

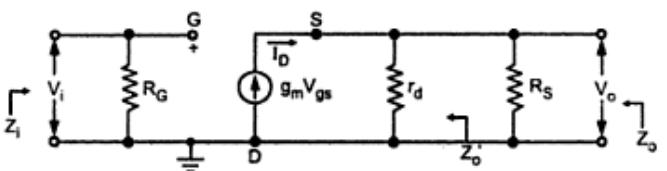


Fig3.13 Simplified small model of Common Drain amplifier

$$Z_i = R_G$$

Output Impedance Z_o

It is given by

$$Z_o = Z'_o \,||\, R_g$$

Where $$Z'_o = \left.\frac{V_o}{I_d}\right|_{V_i = 0}$$

Applying KVL to the outer loop we can have,

$$V_i + V_{gs} - V_o = 0$$

As $V_i = 0,$

$$V_{gs} = V_o$$

Looking at fig. We can write that,

$$g_m V_{gs} = I_d$$

But $V_{gs} = V_o$, so

$$g_m V_o = I_d$$

$$Z_o' = \frac{V_o}{I_d} = \frac{1}{g_m}$$

$$\therefore Z_o = \frac{1}{g_m} \,||\, R_s$$

Voltage gain (A_v)

It is given by

$$A_v = \frac{V_o}{V_i}$$

Looking at Fig. We can write that,

$$V_o = -I_d \left(r_d \,||\, R_s\right)$$

and $$I_d = g_m V_{gs}$$

$\therefore$ $$V_o = -g_m V_{gs} \left(r_d \,||\, R_s\right)$$

But

$$V_i = -V_{gs} + V_o$$

$$= -V_{gs} + \left[-g_m V_{gs} \left(r_d \,||\, R_s\right)\right]$$

Substitute the value Vo and Vi. Then

$$A_V = \frac{-g_m V_{gs}\left(r_d \parallel R_s\right)}{-V_{gs}\left(1+g_m\left(r_d \parallel R_s\right)\right)}$$

$$= \frac{g_m\left(r_d \parallel R_s\right)}{1+g_m\left(r_d \parallel R_s\right)}$$

if $r_d >> R_s$

$$A_v = \frac{g_m R_s}{1+g_m R_s}$$

if $g_m R_s >> 1$

$A_v \approx 1$, but it is always less than one.

Common drain circuit does not provide voltage gain.& there is no phase shift between input and output voltages.

Table summarizes the performance of common drain amplifier

	Exact	$R_d >> R_o$
Z_i	R_G	R_G
Z_o	$\frac{1}{g_m} \parallel R_s$	$\frac{1}{g_m} \parallel R_S$
A_V	$\frac{g_m\left(r_d \parallel R_s\right)}{1+g_m\left(r_d \parallel R_s\right)}$	$\frac{g_m R_s}{1+g_m R_s}$

5. For CS amplifier, the operating point is defined by V_{GSQ} = - 2.5V, Vp = - 6V and I_{dQ} = 2.5mA with I_{DSS} = 8mA, Also R_G = 1M,R_S= 1K Ω ,R_D = 2.2K Ω and V_{DD} = 15V. Calculate g_m, r_d, Z_i, Z_o and A_v. (Nov/Dec 2014)

Given:

V_{GSQ} = -2.5V, V_P = -6V, I_{dQ} = 2.5mA

I_{DSS} = 8mA, R_G = 1M Ω , R_S = 1 K Ω

R_D = 2.2 K Ω , V_{DD} = 15V.

$$g_m = \frac{-2I_{DSS}}{V_p}\left(1-\frac{Vgs}{V_p}\right)$$

$$= \frac{-2\times 8\times 10^{-3}}{-6}\left[1-\left(\frac{-2.5}{-6}\right)\right]$$

$$= 0.00155$$

$$g_m = 1.5\,\text{mA V}^{-1}$$

$$Z_i = R_G = 1\text{M}\Omega$$

$$Z_o = R_D = 2.2\text{K}\Omega$$

$$A_V = g_m R_D$$

$$= 1.5\times 10^{-3}\times 2.2\times 10^{3}$$

$$A_V = 3.3$$

6. Draw the h-parameter model of a BJT – CE amplifier and derive the equations for voltage gain, input impedance and output impedance. (April/may 2015)

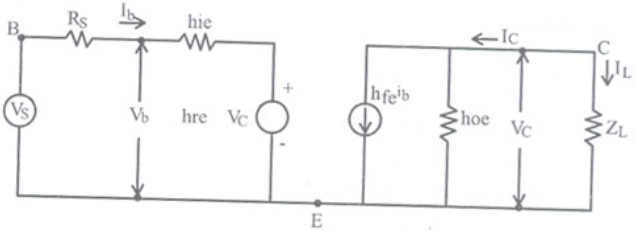


Fig.1. Hybrid Model of a CE Amplifier

Current gain (A_I):

For a transistor amplifier the current gain A_I is defined as the ratio of output current to input current, i.e,

$$A_I = \frac{I_L}{I_b} = \frac{-I_C}{I_b}$$

from figure.1

$$I_C = h_{fe} I_b + h_{oe} V_C$$

Substitute $V_C = I_L Z_L = -I_C Z_L$

$$I_C = h_{fe} I_b - I_C Z_L h_{oe}$$

$$I_C + I_C Z_L h_{oe} = h_{fe} I_b$$

$$I_C \left[1 + Z_L h_{oe}\right] = h_{fe} I_b$$

$$\therefore A_I = \frac{-I_C}{I_b} = \frac{-h_{fe}}{1 + h_{oe} Z_L}$$

$$\therefore A_I = \frac{-h_{fe}}{1 + h_{oe} Z_L} \qquad \text{.....}(1)$$

Input impedance(Z_i):

In the circuit of figure .1 R_S is the signal source resistance. The impedance seen when looking into the amplifier input terminals is the amplifier input impedance Z_i, i.e,

$$Z_i = \frac{V_b}{I_b} \qquad \text{.....}(2)$$

From the input circuit of figure.1

$$V_b = h_{ie} I_b + h_{re} V_C \qquad \text{.....}(3)$$

Substitute equation (3) in (2)

$$Z_i = \frac{h_{ie} I_b + h_{re} V_C}{I_b}$$

$$= h_{ie} + h_{re} \frac{V_C}{I_b} \qquad \text{.....}(4)$$

Substituting,

$$V_C = -I_C Z_L = A_I I_b Z_L \qquad \text{.....}(5)$$

Substitute equation (5) in (4)

$$Z_i = h_{ie} + h_{re} \frac{A_I I_b Z_L}{I_b}$$

$$Z_i = h_{ie} + h_{re} A_I Z_L \qquad \text{.....}(6)$$

Substitute equation (1) in (4)

$$Z_i = h_{ie} - \frac{h_{re} h_{fe}}{1 + h_{oe} Z_L} \qquad \text{.....}(7)$$

The load admittance is $Y_L = 1/Z_L$ Equation written as,

$$Z_i = h_{ie} - \frac{h_{re}h_{fe}}{Z_L\left(h_{oe} + \frac{1}{Z_L}\right)}Z_L$$

$$Z_i = h_{ie} - \frac{h_{re}h_{fe}}{h_{oe} + Y_L} \qquad .....(8)$$

Voltage Gain (A_V):

The ratio of output voltage V_2 input voltage V_1 gives the voltage gain of transistor.

$$A_V = \frac{V_C}{V_b} \qquad .....(9)$$

Substituting $V_C = -I_C Z_L = A_1 I_b Z_L$ in (9)

$$A_V = \frac{A_1 I_b Z_L}{V_b}$$

$$A_V = \frac{A_1 Z_L}{Z_i} \qquad .....(10)$$

Output Admittance, Y_o:

From the circuit of figure.1,

$$I_C = h_{fe}I_b + h_{oe}V_C$$

dividing by V_C

$$\frac{I_C}{V_C} = h_{fe}\frac{I_b}{V_C} + h_{oe} \qquad .....(11)$$

With $v_s = 0$, by KVL in input circuit,

$$R_S I_b + h_{ie}I_b + h_{re}V_C = 0$$

$$\left(R_S + h_{ie}\right)I_b + h_{re}V_C = 0$$

$$\left(R_S + h_{ie}\right)I_b = -h_{re}V_C$$

$$\frac{I_b}{V_C} = \frac{\left(-h_{re}\right)}{R_S + h_{ie}} \qquad .....(12)$$

Substituting equation (12) in (11)

$$\frac{I_C}{V_C} = h_{fe}\frac{(-h_{re})}{R_S + h_{ie}} + h_{oe}$$

$$Y_o = h_{oe} - \frac{h_{fe}h_{re}}{R_S + h_{ie}} \qquad \text{.....(13)}$$

7. Describe about small signal MOFSET amplifier (NMOS) and obtaion the expression for it's transconductance. (April/May 2015)

The small signal model for MOSFET between terminals G, S and D is same as that of JFET. The three basic FET amplifier configurations are:

(i) Common source

(ii) Common drain and

(iii) Common gate.

i) Common Source Amplifier (CS):

A common source amplifier and its small signal equivalent circuit using the voltage source model of FET is shown in figure. 1,(a) and (b) respectively.

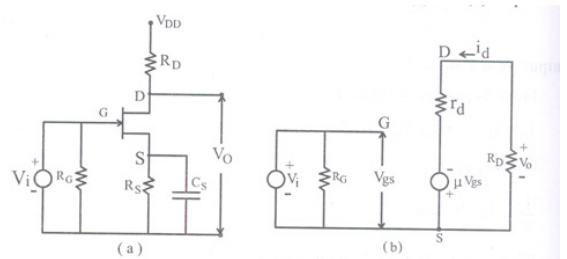


Figure 1. (a) common source amplifier
(b) small signal equivalent circuit of CS amplifier

Voltage gain:

From the small signal equivalent circuit, the output voltage,

$$V_O = \frac{-R_D}{R_D + r_d}\mu V_{gs} \qquad \text{.....(1)}$$

Where $V_{gs} = V_i$ the input voltage,

Hence, the voltage gain,

$$A_V = \frac{V_o}{V_i} = \frac{-\mu R_D}{R_D + r_d} \qquad \text{.....(2)}$$

Input impedance:

From figure. 1, (b) input impedance is given by,

$$Z_i = R_G \qquad \text{.....}(3)$$

Output impedance:

Output impedance is the impedance measured at the output terminals with the input voltage, $V_i = 0$

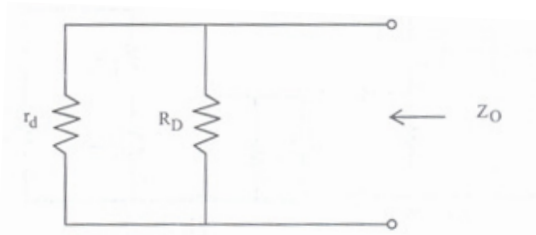


Figure 2 Calculation of output impedance

From figure. 1, (b) when Vi = 0, $V_{gs} = 0$ and hence

$$M\, V_{gs} = 0$$

Then the equivalent circuit for calculating output impedance is given in figure.2,

$$\therefore Z_O = r_d \parallel R_D$$

ii) Common Drain Amplifier (CD):

A single common drain amplifier is shown in figure. 3 (a) and its small signal equivalent circuit using the voltage source model of FET is shown in figure. 3 (b).

The output voltage is determined by the Thevenin's theorem,

$$V_O = \frac{R_s}{R_s + \frac{r_d}{\mu+1}} \times \frac{\mu}{\mu+1} V_{gd}$$

$$V_O = \frac{\mu R_s V_{gd}}{(\mu+1)R_s + r_d} \qquad \text{.....}(4)$$

Where $V_{gd} = V_i$ the input voltage.

Hence , the voltage gain,

$$A_V = \frac{V_o}{V_i} = \frac{\mu R_S}{(\mu+1)R_S + r_d} \qquad .....(5)$$

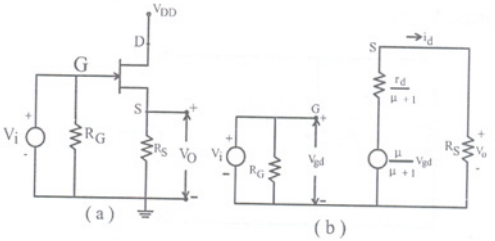


Figure 3. (a) Common drain amplifier
(b) Small signal equivalent circuit of CD amplifier

Input impedance:

From figure.3. (b), input impedance, $Z_i = R_G$ output impedance.

From figure.3. (b) output impedance measured at the output terminals with input voltage $V_i = 0$, i.e.

$$V_i = 0, V_{gd} = 0, \frac{\mu}{\mu+1} V_{gd} = 0$$

Output impedance,

$$Z_o = \frac{r_d}{\mu+1} \| R_S$$

iii) Common Gate amplifier (CG):

A simple common gate amplifier and its small signal equivalent circuit using the current source model of FET is shown in figure. 4 (a) & (b) respectively.

Voltage gain:

By applying KCL,

$$i_r = i_d - g_m V_{gs}$$

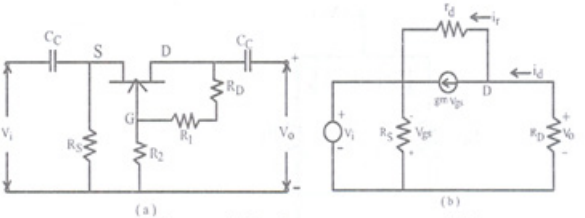


Figure 4. (a) Commom gate amplifier
(b) Small signal equivalent circuit of CG amplifier

Applying KVL around the outer loops,

$$V_o = \left(i_d - g_m V_{gs}\right) r_d - V_{gs}$$

$$\text{But } V_i = -V_{gs} \text{ and } i_d = \frac{-V_o}{R_D}$$

$$\text{Thus } V_o = \left(\frac{-V_o}{R_D} + g_m V_i\right) r_d + V_i$$

Hence the voltage gain,

$$A_A = \frac{V_o}{V_i} = \frac{\left(g_m r_d + 1\right) R_D}{R_d + r_d} \qquad \text{.....}(6)$$

Input impedance:

It is the impedance seen from the output, terminals with input short circuited.

When $V_i = 0$, $V_{gs} = 0$, the output impedance is,

$$Z_o = r_d \parallel R_D$$

UNIT-IV

MULTISTAGE AMPLIFIERS AND DIFFERENTIAL AMPLIFIER

PART - A

1. What is CMRR ? List the methods for improving CMRR?
(April/May 2017, Nov/Dec 2014)

The CMRR is defined as the ratio of differential mode gain to common mode gain.

CMRR=20log Ad/Ac

Methods for improving CMRR

- Using current source circuit instead of RE
- Using current mirror circuit instead of RE
- Using active load i.e. current source circuit as a load

2. What is CMRR? What is it ideal value?
(April/May 2017, Nov/Dec 2015)

The CMRR is defined as the ratio of differential mode gain to common mode gain.

- CMRR=20log Ad/Ac
- The ideal value of CMRR is infinity

3. A tuned circuit has a resonant frequency of 1600 KHz and a band-width of 10 KHz. What is the value of its Q factor?(April/May 2017)

$$B.W = \frac{f_r}{Q}$$

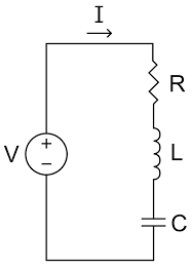
$$Q = \frac{f_r}{B.W}$$

$$Q = \frac{1600KHz}{10KHz} = 160$$

4. What are cascaded amplifiers? (April/May 2015)

A multistage amplifier using two or more single stage common emitter amplifier is called cascaded amplifier

5. Draw the ideal tuned circuit and write the expression for its resonance frequency? (April/May 2015)



$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

6. What is the need for neutralization? (Nov/Dec 2015)

- The technique used to eliminate potential oscillation is neutralization. FET and BJT are unstable
- Over some frequency to overcome it we go for neutralization.

7. Write down the need of cascading the amplifier? (Nov/Dec 2014)

- By cascading amplifiers higher gain is obtained. The overall gain is product of gain of individual stages.
- Cascading is also done to achieve correct input output impedance for specific application

8. What do you mean by tuned amplifiers?

The amplifiers which amplify only selected range of frequencies (narrow band of frequencies) with the help of tuned circuits (parallel LC circuit) are called tuned amplifiers.

9. What are the various types of tuned amplifiers?

1. Small signal tuned amplifiers

   a. Single tuned amplifiers

      - Capacitive coupled
      - Inductively coupled (or) Transformer coupled

   b. Double tuned amplifiers

   c. Stagger tuned amplifiers

2. Large signal tuned amplifiers

10. Give the expressions for the resonance frequency and impedance of the tuned circuit.

$$f_r = \frac{1}{2\pi\sqrt{LC}} \text{ and } Z_r = \frac{L}{CR}$$

11. What is the response of tuned amplifiers?

The response of tuned amplifier is maximum at resonant frequency and it falls sharply for frequencies below and above the resonant frequency.

12. When tuned circuit is like resistive, capacitive and inductive?

- At resonance, circuit is like resistive.
- For frequencies above resonance, circuit is like capacitive.
- For frequencies below resonance, circuit is like inductive.

13. What are the various components of coil losses?

- Copper loss
- Eddy current loss
- Hysteresis loss

14. Define Q factor of resonant circuit.

- It is the ratio of reactance to resistance.
- It also can be defined as the measure of efficiency with which inductor can store the energy.
- Q=2π *(Maximum Energy Stored per cycle / Energy dissipated per cycle)

15. What is dissipation factor?

- It is defined as 1/Q.
- It can be referred to as the total loss within a component.

16. Define unloaded and loaded Q of tuned circuit.

- The unloaded Q or QU is the ratio of stored energy to dissipated energy in a reactor or resonator.
- The loaded Q or QL of a resonator is determined by how tightly the resonator is coupled to its terminations.

17. Why quality factor is kept as high as possible in tuned circuits?

- When Q is high, bandwidth is low and we get better selectivity. Hence Q is kept as high as possible in tuned circuits.
- When Q is high inductor losses are less.

18. List various types of cascaded Small signal tuned amplifiers.

1. Single tuned amplifiers.
2. Double tuned amplifiers.
3. Stagger tuned amplifiers.

19. How single tuned amplifiers are classified?

1. Capacitance coupled single tuned amplifier.
2. Transformer coupled or inductively coupled single tuned amplifier.

20. What are single tuned amplifiers?

Single tuned amplifiers use one parallel resonant circuit as the load impedance in each stage and all the tuned circuits are tuned to the same frequency.

21. What are double tuned amplifiers?

Double tuned amplifiers use two inductively coupled tuned circuits per stage, both the tuned circuits being tuned to the same frequency.

22. What are stagger tuned amplifiers?

Stagger tuned amplifiers use a number of single tuned stages in cascade, the successive tuned circuits being tuned to slightly different frequencies.

(OR)

It is a circuit in which two single tuned cascaded amplifiers having certain bandwidth are taken and their resonant frequencies are adjusted that they are separated by an amount equal to the bandwidth of each stage. Since resonant frequencies are displaced it is called stagger tuned amplifier.

23. What is the effect of cascading single tuned amplifiers on bandwidth? Bandwidth reduces due to cascading single tuned amplifiers.

24. List the advantages and disadvantages of tuned amplifiers.
Advantages:

1. They amplify defined frequencies.

2. Signal to Noise ratio at output is good.

3. They are well suited for radio transmitters and receivers.

4. The band of frequencies over which amplification is required can be varied.

Disadvantages:

1. Since they use inductors and capacitors as tuning elements, the circuit is bulky and costly.

2. If the band of frequency is increased, design becomes complex.

3. They are not suitable to amplify audio frequencies.

25. What are the advantages of double tuned amplifier over single tuned amplifier?

1. It provides larger 3 dB bandwidth than the single tuned amplifier and hence provides the larger gain-bandwidth product.
2. It provides gain versus frequency curve having steeper sides and flatter top.

26. What the advantages are of stagger tuned amplifier?
The advantage of stagger tuned amplifier is to have better flat, wideband characteristics.

27. Mention the applications of class C tuned amplifier.

1. Class C amplifiers are used primarily in high-power, high-frequency applications such as Radio-frequency transmitters.
2. In these applications, the high frequency pulses handled by the amplifier are not themselves the signal, but constitute what is called the Carrier for the signal.

3. Amplitude modulation is one such example.
4. The principal advantage of class-C amplifier is that it has a higher efficiency than the other amplifiers.

28. What i s Neutralization?

The technique used for the elimination of potential oscillations is called neutralization. (OR) The effect of collector to base capacitance of the transistor is neutralized by introducing a signal that cancels the signal coupled through collector base capacitance. This process is called neutralization.

29. What is the use of Neutralization?

1. BJT and FET are potentially unstable over some frequency range due to the feedback parameter present in them.
2. If the feedback can be cancelled by an additional feedback signal that is equal in amplitude and opposite in sign, the transistor becomes unilateral from input to output the oscillations completely stop.
3. This is achieved by Neutralization.

30. What are the different types of neutralization?

1. Hazeltine neutralization
2. Rice neutralization
3. Neutrodyne neutralization.

31. What is rice neutralization?

It uses center tapped coil in the base circuit. The signal voltages at the end of tuned base coil are equal and out of phase.

32. What are the advantages of differential Amplifier?

A differential amplifier helps to increase the CMRR which in turn helps avoid unwanted signals that couple into the input to get propagated. It also helps to increase the signal to noise ratio.

PART – B

1. What is Neutralization ?Explain any one neutralization techniques (April/May 2015)

Neutralization:

TRhe technique used for the elimination of potential oscillation is called **Neutrilization.**

BJT and FET are potentially unstable over some frequency range due to the feedback parameter (Y_N) present in them. If the feedback can be cancelled by an additional feedback signal that is equal in amplitude and opposite in sign, the transistor becomes unilateral from input to output tillthe oscillations completely stop. This is achieved by neutralization.

Hazeltine Neutralization method:

This is a neutralization technique employed in turned RF amplifier to maintain stability.

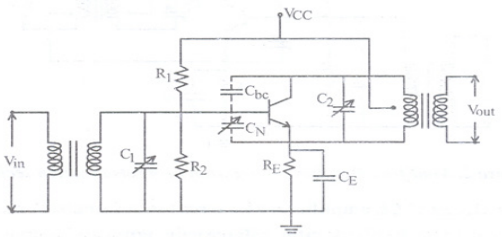


Figure 1. Tuned RF amplifier with Hazeltine Neutralization

In the circuit shown in figure 1, the undesired effect of the collector to base capacitance of the transistor is neutralized by introducing a signal which cancels the signal coupled through the collector to base capacitance.

The figure. 1 shows that a small variable capacitance C_N is connected from the bottom of the coil to the base of the transistor.

The neutralization process is achieved by C_N. It introduces a signal to the base of transistor such that it cancels out the signal fed to the base C_{he}.

Generally a variable capacitor is used for neutralization as the value of C_{he} changes with time. By properly adjusting C_N, exact neutralization is achieved.

In the modified version of Hazeltine neutralization called Neutrodyne neutralization technique, C_N is connected to the lower end of the secondary

coil of the next stage. Hence it is connected with the V_{CC} which ensures that, it is insensitive to any variation in the supply voltage V_{CC} and provides higher stabilization for the tuned amplifier. The circuit for the same is shown in figure 2.

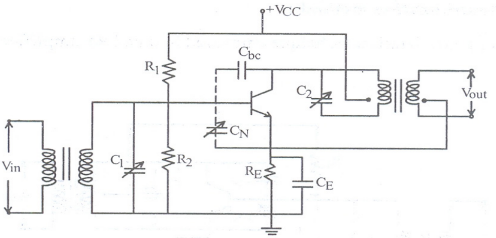


Figure 2. Modified Hazeltine – neutrodyne neutralization technique

2. Draw the circuit of emitter coupled BJT differential amplifier and derive its CMRR (April/May 2015)

The emitter coupled differential amplifier circuit is shown in figure.1

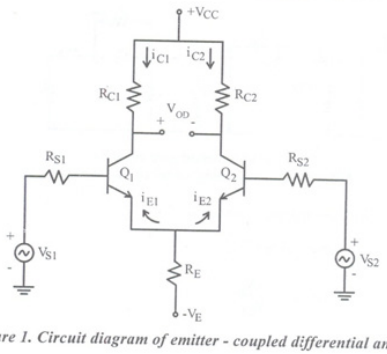


Figure 1. Circuit diagram of emitter - coupled differential amplifier

The a.c. analysis of an emitter – coupled pair:

The differential gain A_d, common mode gain A_C, input and output resistance Ri and R_O can be obtaioned using the h-parameter model.

a)Differential mode gain (A_d):

For analysis, let the two input signals have a magnbitude of $V_S/2$ and differ from each other by 180° phase-shift, as shown in figure. 23. The a.c. equivalent circuit of figure 2 . is shown in figure .3 and a similar structure may be realized for Q3 also.

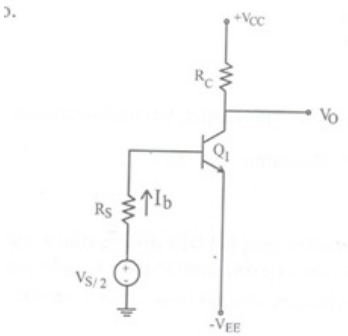


Figure 2. Emitter coupled pair for Ad analysis

Applying KVL loop A 1, the input loop in figure.3

$$I_b\left(R_S + h_{ie}\right) = \frac{V_s}{2}$$

$$I_b = \frac{V_S}{2\left(R_S + h_{ie}\right)}$$

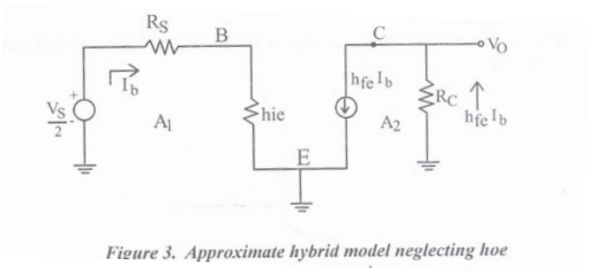


Figure 3. Approximate hybrid model neglecting hoe

Applying KVL to loop A_2, the output voltage is,

$$V_o = -h_{fe} I_b R_C$$

$$\therefore V_o = -h_{fe} R_C \frac{V_S}{2\left(R_S + h_{ie}\right)}$$

$$\frac{V_O}{V_S} = \frac{-h_{fe} R_C}{2\left(R_S + h_{ie}\right)}$$

The minus sign in above equation indicates 180° phase difference between input and output. A sthe magnitude of the input.

As the magnitude of the input signals are equal, $\left(\frac{V_S}{2}\right)$ and are out phase by 180°,.

$$V_{id} = V_1 - V_2 = \frac{V_S}{2} - \left(\frac{V_S}{2}\right) = V_S$$

Therefore, $$A_d = \frac{V_O}{V_{id}} = \frac{V_O}{V_S} = \frac{h_{fe} R_C}{2(R_S + h_{ie})}$$

Where V_S – is the differential input voltage.

(b) Common mode gain (A_C):

Consider the input signals are having the same magnitude V_S and are in same phase.

$$\text{Therefore, } V_C = \frac{V_1 + V_2}{2} = \frac{V_S + V_S}{2} = V_S$$

Unlike, the previous case the emitter current is considered for the analysis the current through R_g is 21_g.

The emitter resistance is assumed to be $2R_g$ and emitter current to be I_g instead of $2I_g$ as shown in figure 4.

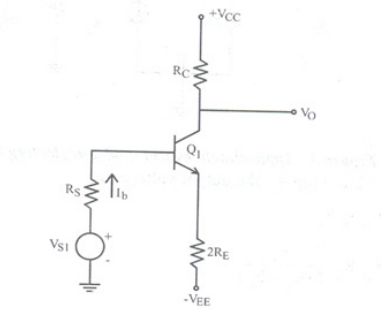


Figure 4. Emitter coupled pair for AC analysis

The approximate hybrid model is shown in figure. 5.

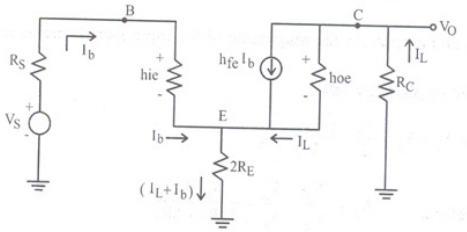


Figure 5. Approximate hybrid model

Current through $R_C = I_L$ (load current)

Effective emitter resistance = $2R_g$

Current through emitter resistance = $I_L + I_D$

Current through $h_{oe} = (I_L - h_{fe} I_b)$

Applying KVL to the input side,

$$I_b R_s + I_b hie + 2R_E (I_L + I_b) = V_S$$

$$\therefore V_S = I_b (R_S + hie + 2R_E) + I_L (2R_E)$$

and $V_o = -I_L R_C$

Apply KVL to output loop,

$$I_L R_C + 2R_E (I_L + I_b) + \frac{I_L - h_{fe} I_b}{hoe} = 0$$

$$I_L R_C + 2R_E I_L + 2R_E I_L + 2R_E I_b + \frac{I_L}{hoe} - \frac{h_{fe} I_b}{hoe} = 0$$

Therefore,

$$I_L \left[R_C + 2R_E + \frac{1}{hoe} \right] = -I_b \left[2R_E - \frac{h_{fe}}{hoe} \right]$$

i.e, $$\frac{I_L}{I_b} = \frac{h_{fe} - 2R_E\, hoe}{1 + hoe(2R_E + R_C)}$$

$$I_b = \frac{I_L (1 + hoe(2R_E + R_C))}{h_{fe} - 2R_E\, hoe}$$

Substituting for I_b,

$$V_S = \frac{I_L\left[1+\text{hoe}\left(2R_E+R_C\right)\right]\left(R_S+\text{hie}+2R_E\right)}{\left(h_{fe}-2R_E\text{hoe}\right)} + I_L\left(2R_E\right)$$

$$\frac{V_S}{I_L} = \frac{\left[1+\text{hoe}\left(2R_E+R_C\right)\left(R_S+\text{hie}+2R_E\right)+2R_E\left(h_{fg}-2R_E\text{hoe}\right)\right]}{h_{fe}-2R_E\ \text{hoe}}$$

Simplifying above equation,

$$\frac{V_S}{I_L} = \frac{\text{hoe}\,R_C\left[R_S+\text{hie}+2R_E\right]+2R_E\left(1+h_{fe}\right)+R_S\left(1+2R_E\ \text{hoe}\right)+\text{hie}\left(1+2R_E\ \text{hoe}\right)}{\left(h_{fe}-2R_E\ \text{hoe}\right)}$$

Rearranging the last two terms in the numerator,

$$\frac{V_S}{I_L} = \frac{\text{hoe}\,R_C\left[2R_E+R_S+\text{hie}\right]+2R_E\left(1+h_{fe}\right)+\left(R_S+\text{hie}\right)\left(1+2R_E\text{hoe}\right)}{\left(h_{fe}-2R_E\text{hoe}\right)}$$

Therefore, $$A_C = \frac{V_O}{V_S} = \frac{-I_L R_c}{V_S}$$

$$AC = \frac{R_C\left(2R_E\ \text{hoe}-h_{fe}\right)}{2R_E\left(1+h_{fe}\right)+\left(R_S+\text{hie}\right)\left(1+2R_E\ \text{hoe}\right)}$$

As shown in figure3, hoe is generally neglected in practical designs,

Therefore,

$$AC = \frac{-R_C\,h_{fe}}{R_S+\text{hie}+2R_E\left(1+h_{fe}\right)}$$

Common Mode Rejection Ratio (CMRR):

$$\text{CMRR} = 20\log\left|\frac{A_d}{A_C}\right|$$

Substituting results of A_d and A_C

$$\text{CMRR} = 20\log_{10}\left|\frac{R_S+\text{hie}+2R_E\left(1+h_{fe}\right)}{R_S+\text{hie}}\right|\text{dB.}$$

3. With neat sketch explain two stage cascaded amplifier and derive its overall A_v, A_i, R_i and R_0 (Nov/Dec 2014)

The most popular cascade amplifier is formed by cascading two CE amplifier stages. Biasing arrangements and coupling elements are omitted for simplicity. The expressions for quantities such as voltage gain, current gain, input impedance and output impedance of this CE amplifier two stage are to be derived using the figure. 1.

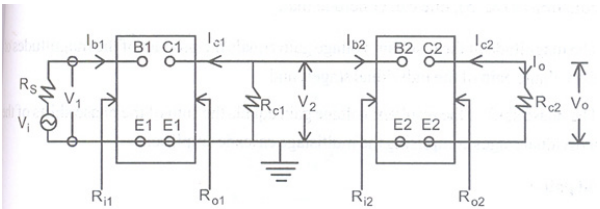


Figure.1. Two stage CE cascaded amplifier

Voltage gain:

The output voltage of first stage acts as the input voltage of second stage. The voltage gain of the complete cascade amplifier is equal to the product of the voltage gains of the individual stages.

The voltage gain of the first stages,

$$\bar{A}_{V1} = \frac{\bar{V}_2}{\bar{V}_1} = \frac{\text{Output voltage of the first stage}}{\text{Input voltage of the first stage}}$$

$$= A_{v1}\underline{|\theta_1} \qquad \text{.....(1)}$$

Where A_{Vi} is the magnitude of voltage gain and θ_1 is phase angle of the output voltage relative to input voltage.

$$\text{similiarly, } \bar{A}_{V2} = \frac{\bar{V}_o}{\bar{V}_2} = A_{V2}\underline{|\theta_2} \qquad \text{.....(2)}$$

The resultant voltage gain,

$$\bar{A}_V = \frac{\bar{V}_o}{\bar{V}_1} = A_V\underline{|\theta} \qquad \text{.....(3)}$$

$$\text{Hence, } A_V = A_{V1} \times A_{V2} \qquad \text{.....(4)}$$

$$\theta = \theta_1 + \theta_2 \qquad \text{.....(5)}$$

For equation (4) & (5), one can conclude that,

(i)The magnitude of the resultant voltage gain equals the product of the magnitudes of the voltage gain of the individual stages, and

(ii)The phase shift of the resultant voltage gain equals the sum of the phase shifts of the individual stages comprisding cascade amplifier.

Current gain:

The current gain,

$$\overline{A}_1 = \frac{\overline{I}_o}{\overline{I}_{b1}} = \frac{\overline{I}_{c2}}{\overline{I}_{b1}}$$

$$\text{Now,} \frac{-\overline{I}_{c2}}{\overline{I}_{b1}} = \frac{-\overline{I}_{c1}}{\overline{I}_{b1}} \cdot \frac{\overline{I}_{c2}}{\overline{I}_{c1}}$$

$$\text{or} \qquad \overline{A}_1 = \overline{A}_{11} . \overline{A}_{12} .$$

$\overline{A}_{11}$ is the base to collector gain of the first stage.

$\overline{A}_{12}$ is the collector to collector current gains of second stage.

Input impedance:

$$R_{in} = h_{ie} + h_{re} \overline{A}_I R_L$$

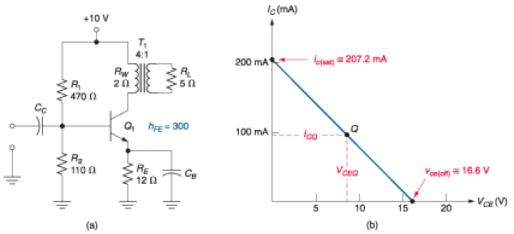
Output impedance:

$$R_0 = 1 / Y_o \qquad \therefore Y_o = h_{oe} - \frac{h_{fe} h_{re}}{h_{ie} + R_S}$$

4. Describe the working of class A and Class C power amplifier in details with relevant diagrams. (April/May 2017)

Transformer-Coupled Class A Amplifiers

A transformer-coupled class A amplifier is shown in Figure below. The transformer is used to couple the amplifier output signal to its load.



A transformer-coupled class A amplifier.

The dc biasing of the transformer-coupled class A amplifier is similar to that of other amplifiers, outside of the fact that the value of V_{CEQ} is designed to be as close as possible to the value of V_{CC}.

Plotting the ac load line of a transformer-coupled class A amplifier, the following are typical characteristics for the transformer-coupled circuit:

- V_{CEQ} is very close to the value of V_{CC}.
- The maximum output voltage is very close to $2V_{CEQ}$ and therefore, can approach the value of $2V_{CC}$.

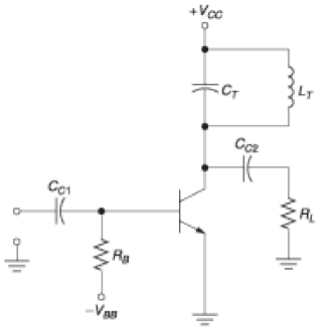
The maximum theoretical efficiency of a transformer-coupled class A amplifier is 50%. In practice, the transformer-coupled amplifier has a value of < 25%. The high theoretical value is a result of assuming that $V_{CEQ} = V_{CC}$ and ignoring transformer (and other) circuit losses.

The transformer-coupled class A amplifier has the following advantages over the RC-coupled circuit:

- Higher efficiency.
- It is relatively simple to match the amplifier and load impedance using a transformer.
- A transformer-coupled circuit can easily be converted to a tuned amplifier; that is, a circuit that provides a specific value of gain over a specified range of operating frequencies.

Class C Amplifiers

The transistor in a class C amplifier conducts for less than 180° of the input cycle. A basic class C amplifier is illustrated in Figure



Class C amplifier.

The most important aspect of the dc operation of this amplifier is that it is biased deeply into cutoff, meaning that $V_{CEQ} \approx V_{CC}$ and $I_{CQ} \approx 0$ A. If a negative supply is used to bias the base circuit, the value of V_{BB} usually fulfills the following relationship:

$$-V_{BB} = 1\ V - V_{in(pk)}$$

The ac operation of the class C amplifier is based on the characteristics of the parallel-resonant tank circuit. If a single current pulse is applied to the tank circuit, the result is a decaying sinusoidal waveform. The waveform shown is a result of the charge/discharge cycle of the capacitor and inductor in the tank circuit, and is commonly referred to as the flywheel effect.

To produce a sine wave that does not decay, we must repeatedly apply a current pulse during each full cycle. At the peak of each positive alternation of the input signal, the tank circuit in a class C amplifier gets the current pulse it needs to produce a complete sine wave at the output. Note that T_1, T_2, and T_3 are inverted at the output relative to the input. This is due to the fact that a common-emitter amplifier produces a 180° voltage phase shift. Note that the bandwidth, Q, and QL characteristics of a class C amplifier are the same as those for any tuned discrete amplifier.

One final point about the class C amplifier. In order for this amplifier to work properly, the tank circuit must be tuned to the same frequency as the input signal, or to some harmonic of that frequency. For instance, you could tune the class C amplifier to the third harmonic of the input and have an output that is three times the input frequency. As such, the class C amplifier can be used as a frequency multiplier.

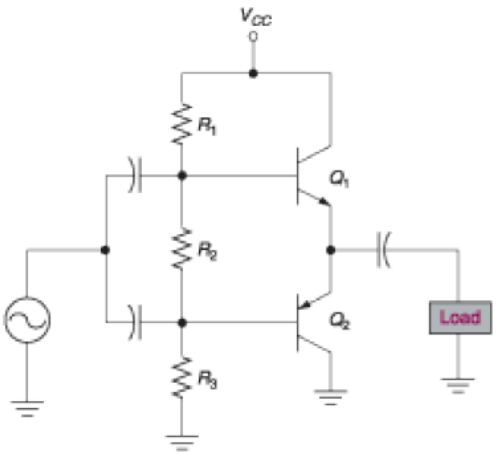
5. Describe the working of class B power amplifier in details with relevant diagrams.

Class B Amplifiers

The class B amplifier is a two-transistor circuit that is designed to improve on the efficiency characteristics of class A amplifiers. A class B amplifier is shown in Figure 11.3. The Q-point values for the circuit in Figure 11.3 are found using

$$V_{ceQ} = \frac{V_{cc}}{2} \quad \text{and} \quad I_{cQ} = I_{co} \cong 0 \text{ A}$$

where ICO is the collector cutoff current rating for the transistor.



Class B amplifier.

The circuit shown in Figure is a complementary-symmetry amplifier, or a push-pull emitter follower. The circuit contains one npn transistor (Q_1) and one pnp transistor (Q_2). The circuit contains complementary transistors; that is, npn and pnp transistors with identical characteristics

6. Explain in detail the methods of coupling Multistage Amplifiers i) RC coupling ii) Transformer coupling and iii) Direct

Coupling.

Solution:

Methods of coupling Multistage Amplifiers

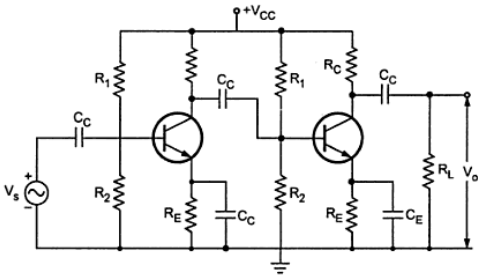
In multistage amplifier, the output signal of preceding stage is to be coupled to the input circuit of succeeding stage. For this interstage coupling,

different types of coupling elements can be employed. These are :

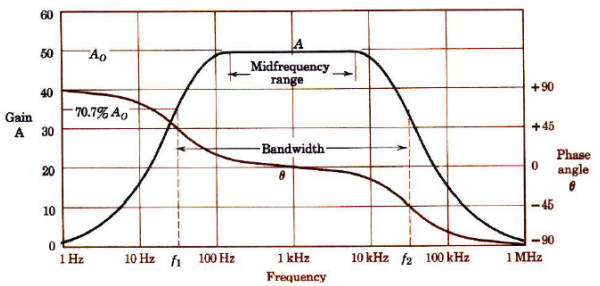
1. RC coupling 2.Transformer coupling 3.Direct coupling

RC coupling

Figure shows RC coupled amplifier using transistors. The output signal of first stage is coupled to the input of the next stage through coupling capacitor and resistive load at the output terminal of first stage

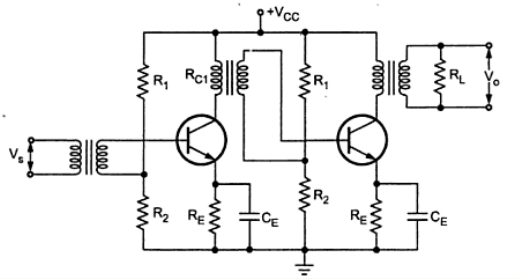


The coupling does not affect the quiescent point of the next stage since the coupling capacitor Cc blocks the d.c. voltage of the first stage from reaching the base of the second stage. The RC network is broadband in nature. Therefore, it gives a wideband frequency response without peak at any frequency and hence used to cover a complete A.F amplifier bands. However its frequency response drops off at very low frequencies due to coupling capacitors and also at high frequencies due to shunt capacitors such as stray capacitance.



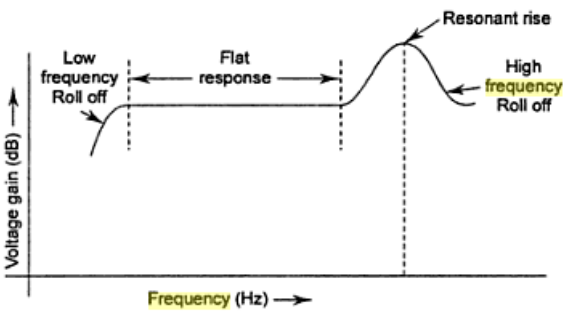
Transformer Coupling

Figure shows transformer coupled amplifier using transistors. The output signal of first stage is coupled to the input of the next stage through an impedance matching transformer



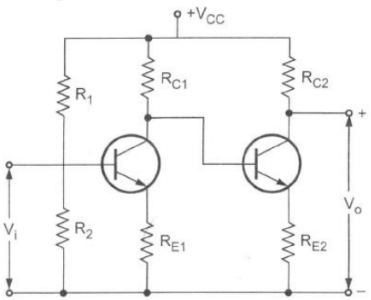
This type of coupling is used to match the impedance between output an input cascaded stage. Usually, it is used to match the larger output resistance of AF power amplifier to a low impedance load like loudspeaker. As we know, transformer blocks d.c, providing d.c. isolation between the two stages. Therefore, transformer coupling does not affect the quiescent point of the next stage.

Frequency response of transformer coupled amplifier is poor in comparison with that an RC coupled amplifier. Its leakage inductance and inter winding capacitances does not allow amplifier to amplify the signals of different frequencies equally well. Inter winding capacitance of the transformer coupled may give rise resonance at certain frequency which makes amplifier to give very high gain at that frequency. By putting shunting capacitors across each winding of the transformer, we can get resonance at any desired RF frequency. Such amplifiers are called tuned voltage amplifiers. These provide high gain at the desired of frequency, i.e. they amplify selective frequencies. For this reason, the transformer-coupled amplifiers are used in radio and TV receivers for amplifying RF signals. As d.c. resistance of the transformer winding is very low, almost all d.c. voltage applied by V_{cc} is available at the collector. Due to the absence of collector resistance it eliminates unnecessary power loss in the resistor.



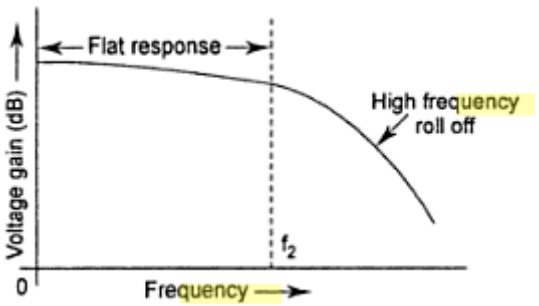
Direct Coupling

Figure shows direct coupled amplifier using transistors. The output signal of first stage is directly connected to the input of the next stage. This direct coupling allows the quiescent d.c. collector current of first stage to pass through base of the next stage, affecting its biasing conditions.



Due to absence of RC components, frequency response is good but at higher frequencies shunting capacitors such as stray capacitances reduce gain of the amplifier.

The transistor parameters such as VBE and β change with temperature causing the collector current and voltage to change. Because of direct coupling these changes appear at the base of next stage, and hence in the output. Such an unwanted change in the output is called drift and it is serious problem in the direct coupled amplifiers.



UNIT-V

FEEDBACK AMPLIFIERS AND OSCILLATORS

PART - A

1. State the Barkhausen criterion for an oscillator. (April/May 2017)

- The total phase shift around a loop, as the signal proceeds from input through amplifier, feedback network back to input again, completing a loop, is precisely 0^O or 360^O.
- The magnitude of the product of the open loop gain of the amplifier (A) and the feedback factor β is unity. i.e.

2. What is meant by feedback?

A portion of the output signal is taken from the output of the amplifier and is combined with the normal input signal. This is known as feedback.

(OR)

Feedback is a part of output is sampled and fedback to the input of the amplifier.

3. Give the different types of feedbacks used in amplifier circuits.

- Positive feedback
- Negative feedback.

4. Define the positive feedback.

When input signal and part of the output signal are in phase, the feedback is calledPositive feedback.

5. Define negative feedback.

When input signal and part of the output signal are in out of phase, the feedback is called negative feedback.

6. Give classification of amplifiers.

The amplifiers can be classified into four broad categories: voltage, current, Tranconductance and Tranresistance amplifiers.

7. What is node sampling?

When the output voltage is sampled by connecting the feedback network in shunt across the output, the connection is referred to as voltage or node sampling.

8. What is loop sampling?

When the output current is sampled by connecting the feedback network in series with the output, the connection is referred to as current or loop sampling.

9. Define feedback factor or feedback ratio.

The ratio of the feedback voltage to output voltage is known as feedback factor or feedback ratio.

10. What is the purpose of mixer network in feedback amplifier?

The mixer network is used to combine feedback signal and input at input of an amplifier.

11. What are the advantages of introducing negative feedback?

1. Input resistance is very high.
2. Output resistance is low.
3. The transfer gain Af of the amplifier with feedback can be stabilized against Variations of the h-parameters or hybrid π parameters of the transistors or the Parameters of the others active devices used in the amplifiers.
4. It improves the frequency response of the amplifiers.
5. There is a significant improvement in the linearity of operation of the feedback.

12. List the four basic feedback topologies.

- Voltage amplifier with voltage series feedback.
- Transconductance amplifier with current-series feedback.
- Current amplifier with current-shunt feedback
- Transresistance amplifier with voltage shunt feedback

13. Give the expression for gain of an amplifier with feedback.

$A_{vf} = A_V / 1 + A_V \beta$

Where, A_{vf} – feedback voltage gain.

A_V – Voltage gain.

β - Feedback factor

14. What is loop gain or return ratio.

A path of a signal from input terminals through basic amplifier, through the feedback network and back to the input terminals forms a loop. The gain of this loop is the product $-A\beta$. This gain is known as loop gain or return ratio.

15. What is sensitivity of the transfer gain?

The fractional change in amplification with feedback divided by the fractional change without feedback is called the sensitivity of the transfer gain.

16. What is desensitivity?

The reciprocal of the sensitivity is called the desensitivity D. it is given as $D = 1 + A\beta$

17. What is the effect of lower cut-off frequency with negative feedback?

Lower cutoff frequency with feedback is less than lower cutoff frequency without feedback by factor (1+Amid β)

18. What is the effect of upper cut-off frequency with negative feedback?

Upper cutoff frequency with feedback is greater than upper cutoff frequency without feedback by factor (1+Amid β)

19. What is the effect of negative feedback on bandwidth?

Bandwidth of amplifier with feedback is greater than bandwidth of amplifier without feedback.

20. What is the effect of negative feedback on feedback distortion?

The frequency distortion is reduced with the negative feedback.

21. Why gain bandwidth product remains constant with the introduction of negative feedback?

Since bandwidth with negative feedback increases by factor (1+A β) and gain decreases by same factor, the gain-bandwidth product of an amplifier does not altered, when negative feedback is introduced.

22. What is the effect of negative feedback on noise?

The noise is reduced with the negative feedback.

23. What is the effect of negative feedback on non linear distortion?

The linear distortion is reduced with the negative feedback.

24. What are the types of distortions in an amplifier?

- Frequency
- Noise and non linear

25. What type of feedback is employed in emitter follower amplifier?

Voltage series feedback.

26. A feedback amplifier has an open loop gain of 600 and feedback factor β = 0.01. Find the closed loop gain with feedback.

$$A_{vf} = A_V / 1 + A_V \beta$$

$$= 600/(1 + 600*0.01)$$

$$= 85.714.$$

27. The distortion in an amplifier is found to be 3%, when the feedback ratio of negative feedback amplifier is 0.04. When the feedback is removed, the distortion becomes 15%. Find the open and closed loop gain.

Solution:

Given: $\beta = 0.04$

Distortion with feedback = 3%,

Distortion without feedback = 15%

$D = 15/3 = 5.$

Where $D = 1 + A\beta = 5$

$A = 100.$

28. Which is the most commonly used feedback arrangement in cascaded amplifiers and Why?

Voltage series feedback is the most commonly used feedback arrangement in cascaded amplifiers. Voltage series feedback increases input resistance and decreases output resistance. Increase in input resistance reduces the loading effect of previous stage and the decrease in output resistance reduces the loading effect of amplifier itself for driving the next stage.

29. Voltage gain of an amplifier without feedback is 60dB. It decreases to 40dB with feedback. Calculate the feedback factor.

Solution:

Given: $A_v = 60$dB and $A_{vf} = 40$ dB. We know that,

$A_{Vf} = A_V / 1 + A_V\beta$

$\beta = (A_V - A_{vf}) / (A_V A_{vf})$

$= (60-40) / (60*40)$

$\beta = 0.00833.$

30. State the nyquist criterion for stability of feedback amplifiers?

- The amplifier is unstable if the curve encloses the point -1+j0. The system is called as unstable system.
- The amplifier is stable if the curve encloses the point -1+jo. That system is called as stable system.

31. What is nyquist diagram?

The plot which shows the relationship between gain and phase-shift as a function of frequency is called as nyquist diagram.

32. Write the steps which are used to identify the method of feedback topology?

- Identify topology (type of feedback)
  - i) To find the type of sampling network.
  - ii) To find the type of mixing network
- Find the input circuit.
- Find the output circuit.

- Replace each active device by its h-parameter model at low frequency.
- Find the open loop gain (gain without feedback), A of the amplifier.
- Indicate X_f and X_o on the circuit and evaluate $\beta = XfXO$.
- Calculate A, and β, find D, Ai, Rif, Rof and Rof'.

33. Write down the various characteristics of topology?

Characteristics	Topology			
	Voltage series	Current series	Current shunt	Voltage shunt
Sapling signal, XO	Voltage	Voltage	Current	Current
Mixing signal	Voltage	Current	Current	Voltage
To find input loop, Set	$V_0=0$	$I_0=0$	$I_0=0$	$V_0=0$
to find output loop, set	$I_i=0$	$I_i=0$	$V_i=0$	$V_I=0$
Signal source	Thevenin	Thevenin	Norton	Norton
$\beta = X_f/X_0$	V_f/V_0	V_f/I_0	I_f/I_0	I_f/I_0
$A=X_0/X_i$	$A_V=V_0/V_i$	$G_M=I_0/V_i$	$A_I=I_0/I_i$	$R_M=V_0/I_i$
$D=1+\beta A$	$1+\beta A_v$	$1+\beta G_M$	$1+\beta A_I$	$1+\beta R_M$
Af	AV/D	GM/D	AI/D	RM/D
R_{if}	R_iD	R_iD	R_i/D	R_i/D
R_{Of}	$R_0/(1+\beta A_V)$	$R_0(1+\beta G_M)$	$R_0(1+\beta A_I)$	$R_0/(1+\beta R_M)$
R_{Of}'	$R_0'/(1+\beta A_V)$	$R_0(1+\beta A_V)/(1+\beta A_V)$	$R_0(1+\beta A_V)/(1+\beta A_V)$	$R_0'/(1+\beta R_M)$

34. What is an oscillator?

An oscillator is a circuit which basically acts as a generator, generating the output signal which oscillates with constant amplitude and constant desired frequency.

35. Why in practice A β is kept greater than unity.

To amplify small noise voltage present, so that oscillations can start, A β is kept initially greater than unity.

36. What is the difference between open loop and closed loop gain of the circuit?

S.No	Open loop gain	Closed loop gain
1.	The gain of the amplifier is ratio of output to input when no feedback is used is called open loop gain	The ratio of the output to input, considering the overall effect of the feedback is called closed loop gain.

37. Explain the concept of positive feedback.

The feedback is a property which allows to feedback the part of the output, to the same circuit as its input. Such a feedback is said to be positive whenever the part tf the output that is fed back to the amplifier as its input, is in phase with the original input signal applied to the amplifier.

38. From where starting voltage for the oscillator is derived?

Every resistance has some free electrons. Under the influence of room temperature, these free electrons move randomly in various directions. In such a movement of the free electrons generate a voltage called noise voltage, across the resistance. Such noise voltage provides the starting voltage for the oscillator.

39. Give the over all classification of oscillators?

- Waveform type (sinusoidal, square, triangular,etc.,)
- Circuit components (LC, RC,etc.,)
- Range of frequency –A.F (audio), R.F (radio)
- Type of feedback (RC phase shift, Wein bridge are feedback used, UJT relaxation oscillators uses no feedback)

40. What are the frequency sensitive arms?

The arms which decide the frequency of oscillations i.e., R_1-C_1 and R_2-C_2 are the frequency sensitive arms.

41. What is the gain requirement in the wein bridge oscillator?

The gain requirement for wein bridge oscillator is minimum 3.

42. How to obtain Hartley oscillator from the basic form of LC oscillator

Using X_1 and X_2 as inductors and X_3 as capacitor, Hartley oscillator from basic form of LC oscillator is obtained.

43. How to obtained colpitt's oscillator form basic form of LC oscillator?

Using X_1 and X_2 as capacitors and X_3 as inductors, colpitt's oscillator from basic form of LC oscillator is obtained.

44. Write down the advantages of RC phase shift oscillator.

- Simplicity of the circuit.
- Useful for frequencies in the audio range.
- A sine wave output can be obtained.

45. Write down disadvantages of RC phase shift oscillator.

- Poor frequency stability.
- It is difficult to get a variable frequency output, because to change the frequency, we need to vary all the resistors and capacitors simultaneously which is practically very difficult.

46. Write down the advantages, disadvantages and applications of Hartley oscillator.

Advantages:

- It is easy to tune
- It can operate over a wide frequency typically from few Hz and several MHz.
- It is easy to change the frequency by means of a variable capacitor.

Disadvantages:

- Poor frequency stability.

Applications:

- It is used as local oscillator in radio and TV receivers.
- In the function generator.
- In RF sources

47. Write down the advantages, disadvantages and applications of colpitt's oscillator.

Advantages:

- Simple construction.
- It is possible to obtain oscillations at very high frequencies.

Disadvantages:

- It is difficult to adjust the feedback as it demands change in capacitor values.
- Poor frequency stability.

Application:

- As a high frequency generator.

48. Write down the comparison between LC oscillators and crystals oscillators.

S.No	Crystal oscillator	LC oscillator
1.	Frequency of oscillations depends on the dimensions of crystal	Frequency of oscillations is dependent on values of L and C
2.	Accuracy depends only on the fine cut of the crystal	Accuracy mainly depends on tolerances of L and C
3.	Q is very high and it is stable	Q is less as compared to the crystal
4.	Miller crystal oscillator, pierce crystal oscillator are the examples of crystal oscillator	Hartley, Colpitt's and clap oscillators are the examples of LC oscillators.

49. Write down the advantages, disadvantages andapplications of crystal oscillator.

Advantages:

- Very high frequency stability.
- Very low frequency drift due to change in temperature and other parameters.
- It is possible to obtain very high, precise and stable frequency of oscillations.

- The Q is very high.

Disadvantages:

- These are suitable for high frequency applications.
- Crystals of low fundamental frequencies are not easily available.

Applications:

- As a crystal clock in microprocessors.
- In the frequency synthesizers.
- In the radio and TV transmitters.
- In special types of receivers.

50. Give the comparison between RC and LC oscillators.

S.No	RC oscillators	LC oscillators
1.	Frequency of oscillations is dependent on values of R and C	Frequency of oscillations is dependent on values of L and C
2.	These are used at low and medium frequencies	These are preferred at high frequencies
3.	Phase shift and wein bridge oscillators are the examples of RC oscillators	Hartley, colpitt's and clapp oscillators are the examples of LC oscillators

51. Write down the general applications of oscillators.

- As a local oscillator in radio receivers.
- In T.V receivers.
- In signal generators.
- As clock generation for logic circuits.
- AM and FM transmitters.
- In phase lock loops.

52. Write down the comparison of RC oscillators.

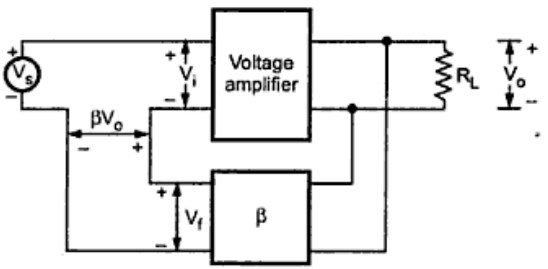
S.No	Parameter	Phase shift oscillator	Wein bridge oscillator
1.	Feedback network	Consists of three identical RC sections connected in cascade	Uses wien bridge circuit as feedback network
2.	Phase shift introduced by the feedback network	180^0 at frequency of oscillations	0^o at frequency of oscillations
3.	Phase shift introduced by the amplifier	180^0 at frequency of oscillations	0^o at frequency of oscillations
4.	Frequency of oscillations	$f_0 = \frac{1}{2\pi\sqrt{6RC}}$	$f_0 = \frac{1}{2\pi RC}$
5.	Value of β	β = -1/29 for oscillator using OP-AMP	β = + 1/3 for oscillator using OP- AMP
6.	minimum value of gain	$A \geq 29$ for sustained oscillations	$A \geq 3$ for sustained oscillations
7.	Variable output frequency	Possible but difficult	Possible and easy
8.	Amplitude or gain stabilization	Necessary	Necessary

PART B

1. Briefly explain voltage series feedback amplifier with neat diagram and derive an expression for input and output resistance.

(April/May 2017, Nov/Dec 2016)

The fig shows the block diagram of voltage series feedback amplifier. A sample of output voltage i.e., $V_f = \beta V_0$ is connected in series opposition to the input voltage signal V_S. The gain of the amplifier with feedback is as follows:



We have seen, the symbol A is used to represent trasnfer gain of the basic amplifier without feedback and symbol A_f is used to represent transfer gain of the basic amplifier with feedback. These are given as,

$$A = \frac{X_o}{X_i} \text{ and } A_f = \frac{X_o}{X_s}$$

Where X_o = Output voltage or output current

X_i = Input voltage or input current

X_s = Source voltage or source current

As it is a negative feedback the relation between X_i and X_s is given as,

$$X_i = X_s + (-X_f)$$

Where X_f = Feedback voltage or feedback current

$$\therefore \quad A_f = \frac{X_o}{X_s} = \frac{X_o}{X_i + X_f}$$

Dividing by X_i to numerator and denominator we get,

$$A_f = \frac{X_o / X_i}{(X_i + X_f)/X_i}$$

$$= \frac{A}{1 + X_f / X_i} \quad \because A = \frac{X_o}{X_i}$$

$$= \frac{A}{1 + (X_f / X_o)(X_o / X_i)}$$

$$\therefore \quad A_f = \frac{A}{1 + \beta A} \qquad \because \beta = \frac{X_f}{X_o} \qquad \text{.....}(1)$$

Where β is a feedback factor.

Looking at equation we can say that gain without fdeedback (A) is always greater than gain without feedback (A/(1 + βA) and it decrease with increase in β i.e. increase in feedback factor.

For voltage amplifier, gain with negative feedback is given as ,

$$A_{vr} = \frac{A_v}{1 + A_v \beta} \qquad \text{.....}(2)$$

Where A_V = Open loop gain i.e. gain without feedback

B = Feedback Factor

Input Resistance:

If the feedback signal is added to the input in series with the applied voltage (regardless of whether the feedback is obtained by sampling the output current or voltage), it increases the input resistance. Since the feedback voltage V_f opposes V_s, the input current I_i is less than it would be if V_f were absent, as shown in the fig. 3.11.

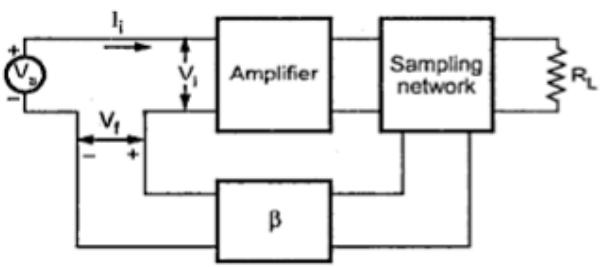


Fig. 3.11

Voltage series feedback:

The voltage series feedback topology shown in Fig. 3.13 with amplifier is replaced by Thevenin's model. Here, A_v represents the open circuit voltage gain taking R_s into account. Since throughout the discussion of feedback amplifiers we will consider R_S to be part of the amplifier and we will drop the subjected on the transfer gain input resistance (A_V instead of A_{vs} and R_{if} instead of R_{ifs}).

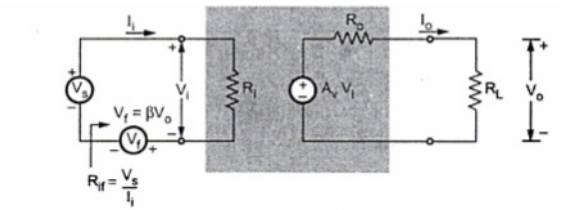


Fig. 3.13

Look at Fig. 3.13 the input resistance with feedback is given as,

$$R_{if} = \frac{V_S}{I_i} \qquad \text{.....(18)}$$

Applying KVL to the input side we get,

$$V_S - I_i R_i - V_f = 0$$

$$\therefore \quad V_S = I_i R_i + V_f$$

$$= I_i R_i + \beta V_o \qquad \text{.....(19)}$$

The output Voltage V_o is given as,

$$V_o = \frac{A_v V_i R_L}{R_o + R_L}$$

$$= A_V I_i R_i = A_V V_i \qquad \text{.....(20)}$$

where $$A_V = \frac{V_o}{V_i} = \frac{A_v R_L}{R_o + R_L}$$

Key Points: A_v represents the open circuit voltage gain without feedback and A_V is the voltage gain without feedback taking the load R_L into account.

Substituting value of V_O from equation (20)in equation (19) we get,

$$V_s = I_i R_i + \beta A_v I_i R_i$$

$$\therefore \quad \frac{V_s}{I_i} = R_i + \beta A_v R_i$$

$$\therefore \quad R_{if} = R_i (1 + \beta A_V) \qquad \text{.....(21)}$$

Output Resistance:

The negative feedback which samples the output voltyage, regardless of how this output signal is returned to the input, lends to decrease the output resistance, as shown in the fig. 3.17.

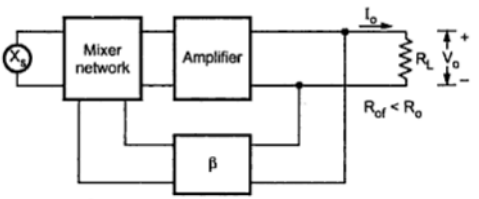


Fig. 3.17

On the other hand, the negative feedback which samples the output current, regardless of how this output signal is returned to the input, tends to increase the output resistance, as shown in the Fig. 3.18.

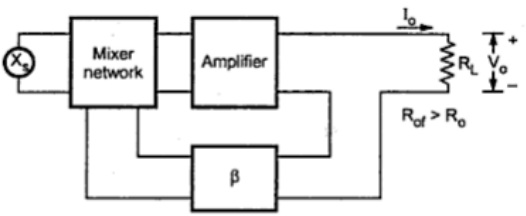


Fig. 3.18

Now, we see the effect of negative feedback on output resistance in different topologies (ways) of introducing negative feedback and obtain R_{of} quantitatively.

Voltage series feedback:

In this topology, the output resistance can be measured by shorting the input source V_S =0 and looking into the output terminals with R_L disconnected, as shown in the Fig. 3.19.

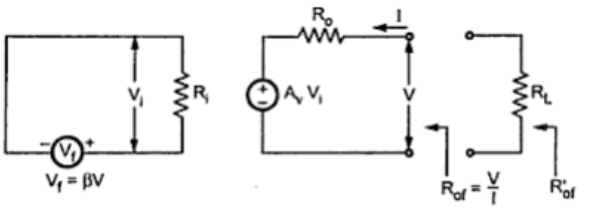


Fig. 3.19

Applying KVL to the output side we get,

$$A_v V_i + IR_o - V = 0$$

$$\therefore \quad I = \frac{V - A_v V_i}{R_o} \qquad .....(31)$$

The input voltage is given as,

$$V_i = -V_f = -\beta V \quad \because V_s = 0$$

Substituting the V_i from equation (32) in equation (31) we get,

$$I = \frac{V + A_v \beta V}{R_o}$$

$$= \frac{V(1 + \beta A_v)}{R_o}$$

$$\therefore \quad R_{of} = \frac{v}{I}$$

$$= \frac{R_o}{(1 + \beta A_v)} \qquad .....(33)$$

Key point: Here A_v is the open loop voltage gain without taking nR_L in account.

$$R'_{of} = R_{of} \parallel R_L$$

$$= \frac{R_{of} \times R_L}{R_{of} + R_L} = \frac{\left(\frac{R_o}{1 + \beta A_v}\right) \times R_L}{\frac{R_o}{(1 + \beta A_v)} + R_L}$$

$$= \frac{R_o R_L}{R_o + R_L(1 + \beta A_v)} = \frac{R_o R_L}{R_o + R_L + \beta A_V R_L}$$

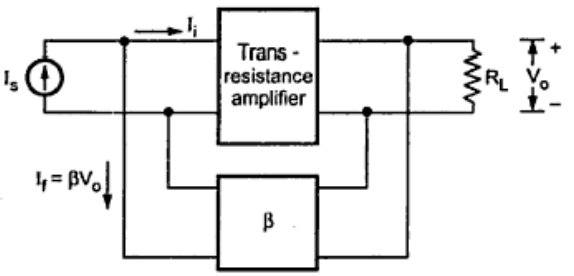
Dividing numerator and denominator by $(R_o + R_L)$ we get

$$R'_{of} = \frac{\frac{R_o R_L}{R_o + R_L}}{1 + \frac{\beta A_v R_L}{R_o + R_L}}$$

$$= \frac{R'_o}{1 + \beta A_v} \quad \because R'_o = \frac{R_o R_L}{R_o + R_L} \text{ And } A_v = \frac{A_v R_L}{R_o + R_L} \qquad .....(34)$$

Key Point: Here A_v is the open loop voltage gain taking R_L into account.

2. Briefly explain voltage shunt feedback amplifier with neat diagram and derive an expression for input and output resistance.



If the feedback signal is added to the input in shunt with the applied voltage (regardless of whether the feedback is obtained by sampling the output voltage or current), it decreases the input resistance

Since $I_S = I_i + I_f$ the current I_S drawn from the signal source is increased over what it would be if there were no feedback current as shown in the fig.

Hence, the output resistance with feedback $R_{if} = \frac{V_i}{I_s}$ is decreased for the circuit shown in fig.

Voltage shunt feedback:

The voltage shunt feedback topology is shown in Fig. 3.16 with amplifier input circuit is represented by Norton's equivalent circuit and output circuit represented by Thevenin's equivalent .

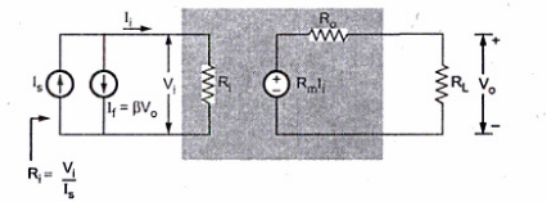


Fig. 3.16

Applying KCL at input node we get,

$$I_S = I_i + I_f$$
$$= I_i + \beta V_o \qquad \ldots\ldots\ldots(28)$$

The output voltage V_o is given as,

$$V_o = \frac{R_m I_i R_o}{R_o + R_L}$$
$$= R_M I_i \qquad \ldots\ldots\ldots(29)$$

where $$R_M = \frac{R_m R_o}{R_o + R_L}$$

Key Point: R_m represents the open circuit transresistanmce without fedback and R_M is the transresistance without feedback taking the load R_L into account.

Substituting Value of V_o from equation (29) into equation (28) we get,

$$I_B = I_i + \beta R_M I_i$$
$$= I_i (1 + \beta R_M)$$

The resistance with feedback R_{if} is given as,

$$R_{if} = \frac{V_i}{I_s} = \frac{v_i}{I_i (1 + \beta R_M)}$$

$$\therefore \quad R_{if} = \frac{R_i}{(1 + \beta R_M)} \quad \because R_i = \frac{V_i}{I_i} \qquad \ldots\ldots\ldots(30)$$

Output Resistance:

Voltage shunt feedback:

In this topology, the output resistance can be measured by shorting the input source $V_S = 0$ and looking into the output terminals with R_L disconnected, as shown in the Fig. 3.20.

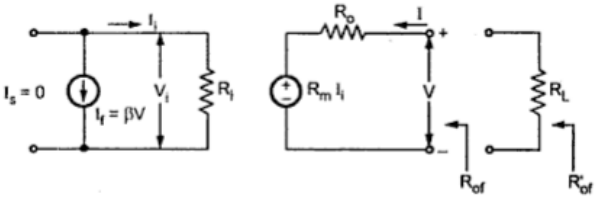


Fig. 3.20

Applying KVL to the output side we get,

$$R_m I_i + I R_o - V = 0$$

$$\therefore \quad I = \frac{V - R_m I_i}{R_o} \qquad \text{.....(35)}$$

The input current is given as,

$$I_i = -I_f = -\beta V \qquad \text{.....(36)}$$

Substituting I_i from equation (36) in equation (35) we get,

$$I = \frac{V + R_m \beta V}{R_o} = \frac{V(1 + R_m \beta)}{R_o}$$

$$\therefore \quad R_{of} = \frac{V}{I}$$

$$= \frac{R_o}{1 + R_m \beta} \qquad \text{.....(37)}$$

Key Point: Here, R_m is the open loop transresistance without taking R_L in account.

$$R'_{of} = R_{of} \,||\, R_L = \frac{R_{of} \times R_L}{R_{of} + R_L}$$

$$= \frac{\dfrac{R_o \times R_L}{1 + R_m \beta}}{\dfrac{R_o}{1 + R_m \beta} + R_L} = \frac{R_o R_L}{R_o + R_L (1 + R_m \beta)}$$

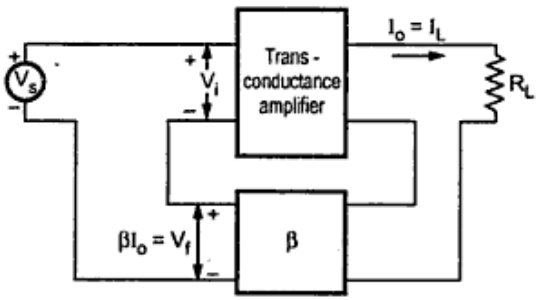
Dividing numerator and denominator by $R_o + R_L$ we get,

$$R'_{of} = \frac{\dfrac{R_o R_L}{R_o + R_L}}{1 + \dfrac{\beta R_m R_L}{R_o + R_L}}$$

$$= \frac{R'_o}{1 + \beta R_m} \quad \because R'_o = \frac{R_o R_L}{R_o + R_L} \text{ and } R_M = \frac{R_m R_L}{R_o + R_L} \qquad \text{.....(38)}$$

Key point: Here R_M is the open loop transresistance taking R_L in account.

3. Briefly explain current series feedback amplifier with neat diagram and derive an expression for input and output resistance.



Transconductance amplifier with current series feedback

Current Series feedback:

The current series feedback topology is shown in Fig. 3.14 with amplifier input circuit is represented by Thevenin's equivalent circuit and output circuit by Norton's equival;ent circuit.

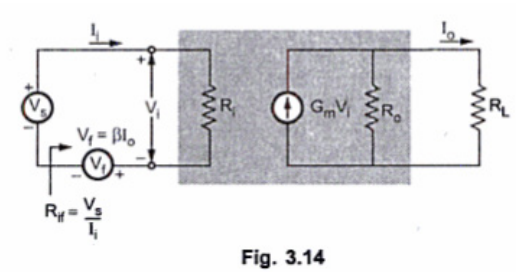


Fig. 3.14

Looking at fig. 3.14 the input resistance with feedback is given as,

$$R_{if} = \frac{V_s}{I_i}$$

Applying KVL to the input side we get,

$$V_S - I_i R_i - V_f = 0$$

$$\therefore \quad V_s = I_i R_i + V_f = I_i R_i + \beta I_o \qquad \text{.....}(22)$$

The output current I_o is given as,

$$I_o = \frac{G_m V_i R_o}{R_o + R_L} = G_M V_i \qquad \text{.....}(23)$$

Where

$$G_M = \frac{I_o}{V_i}$$

$$G_M = \frac{G_m R_o}{R_o + R_L}$$

Key Point: G_m represents the open circuit transconductance without feedback and G_m is the transconductance without feedback taking the load R_L into account.

Substituting value of I_O from equation (23) into equation (22) we get,

$$V_s = I_i R_i + \beta G_M V_i$$
$$= I_i R_i + \beta G_M I_i R_i \qquad \because V_i = I_i R_i$$

$$\therefore \qquad \frac{V_S}{I_i} = R_i\left(1 + \beta G_M\right)$$

$$\therefore \qquad R_{if} = \frac{V_s}{I_i} = R_i\left(1 + \beta G_M\right) \qquad .....(24)$$

Current Series feed back:

In this topology the output resistance can be measured by shorting the input source $V_S = 0$ and looking into the output terminals with R_L disconnected, as shown in the Fig. 3.22

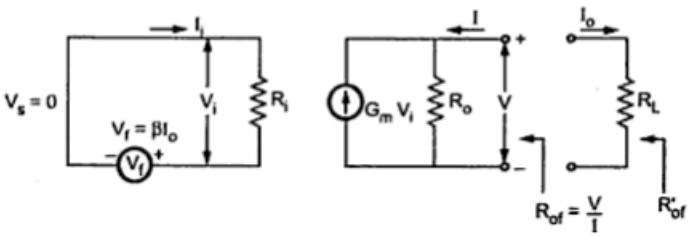


Fig. 3.22

Applying KCL to the output node we get,

$$I = \frac{V}{R_o} - G_m V_i \qquad .....(43)$$

The input Voltage given as,

$$V_i = -V_f = -\beta I_o$$
$$= \beta I \quad \because I_o = -I \qquad .....(44)$$

Substituing value of V_i from equation (44) in equation (43) we get,

$$I = \frac{V}{R_o} - G_m \beta I$$

$$\therefore I(1 + G_m\beta) = \frac{V}{R_o}$$

$$\therefore \quad R_{of} = \frac{v}{I} = R_o(1 + G_m\beta) \qquad .....(45)$$

Key Point: Here, G_m is the open loop transconductance without taking R_L in account.

$$R'_{of} = R_{of} \,||\, R_L = \frac{R_{of} \times R_L}{R_{of} + R_L}$$

$$= \frac{R_o(1+\beta G_m)R_L}{R_o(1+\beta G_m) + R_L} = \frac{R_o R_L(1+\beta G_m)}{R_o + R_L + \beta G_m R_o}$$

Dividing numerator and denominator by $R_o + R_L$ we get,

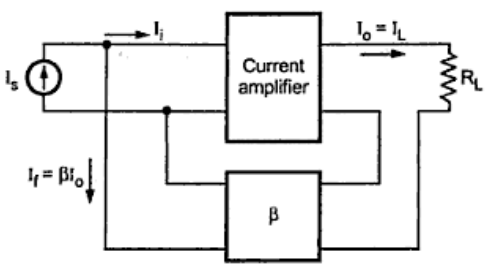
$$R'_{of} = \frac{\dfrac{R_L R_o(1+\beta G_m)}{R_o + R_L}}{1 + \dfrac{\beta G_m R_o}{R_o + R_L}}$$

$$= \frac{R'_o(1+\beta G_m)}{1+\beta G_m} \because R'_o = \frac{R_o R_L}{R_o + R_L} \text{ and } G_M = \frac{G_m R_o}{R_o + R_L} \qquad .....(46)$$

Key Point: Note that here, G_M is the open loop current gain taking R_L in account.

4. Briefly explain current shunt feedback amplifier with neat diagram and derive an expression for input and output resistance.

(April/May 2017)



Current amplifier with current shunt feedback

Current shunt feedback:

The current shunt feedback topology is shown in Fig. 3.15 with amplifier input and output replaced by Nortion's equivalent circuit.

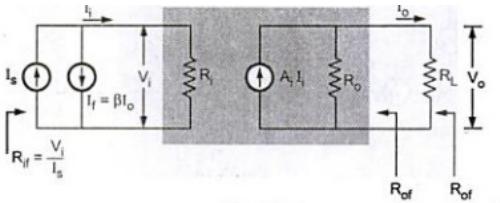


Fig. 3.15

Applying KCL to the input node we get,

$$I_o = I_i + I_f$$
$$= I_i + \beta I_o \qquad \text{..... } (25)$$

The output I_o is given as,

$$I_o = \frac{A_i I_i R_o}{R_o + R_L}$$
$$= A_i I_i \qquad \text{.....}(26)$$

where $$A_i = \frac{A_i R_o}{R_o + R_i}$$

Key Point: A_i represents the open circuit gain without feedback and A_1 is the current gain without feedback taking the load R_L into account.

Substituting Value of I_o from equation (26) into equation (25) we get,

$$I_o = I_i + \beta A_1 I_i$$
$$= I_i (1 + \beta A_1)$$

The input resistance with feedback is given as,

$$R_{if} = \frac{V_i}{I_o} = \frac{V}{I_i (1 + \beta A_1)}$$
$$= \frac{R_i}{(1 + \beta A_t)} \qquad \because R_i = \frac{V_i}{I_i} \qquad \text{.....}(27)$$

Current shunt feedback:

In this topology, the output resistance can be measured by open circuiting the input source $I_s = 0$ and looking into the output terminals, with R_L disconnected, as shown in the Fig. 3.21.

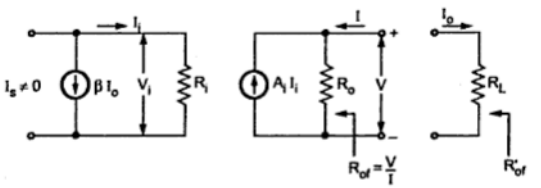


Fig. 3.21

Applying the KCL to the output node we get,

$$I = \frac{V}{R_o} - A_i I_i \qquad \text{.....}(39)$$

The input is given as,

$$I_i = -I_f = -\beta I_o \quad \because I_s = 0$$
$$= \beta I \quad \because I = -I_o \qquad \text{.....}(40)$$

Substituting value of I_i from equation (40) in equation (39) we get,

$$I = \frac{V}{R_o} - A_i \beta I$$

$$\therefore \quad I(1 + A_i\beta) = \frac{V}{R_o}$$

$$\therefore \quad R_{of} = \frac{V}{I} = R_o(1 + \beta A_i) \qquad \text{.....}(41)$$

Key Point: Here, A_i is the open loop current gain without taking R_L in account,

$$R'_{of} = R_{of} \parallel R_L = \frac{R_{of} \times R_L}{R_{of} + R_L}$$
$$= \frac{R_o(1 + \beta A_i)R_L}{R_o(1 + \beta A_i) + R_L} = \frac{R_o R_L (1 + \beta A_i)}{R_o + R_L + \beta A_i R_o}$$

Dividing numerator and demoniator by $R_o + R_L$ we get,

$$R'_{of} = \frac{\dfrac{R_o R_L (1+\beta A_i)}{R_o + R_L}}{1+\dfrac{\beta A_i R_o}{R_o + R_L}} = \frac{R'_o (1+\beta A_i)}{(1+\beta A_i)}$$

$$\because \quad R'_o = \frac{R_o R_L}{R_o + R_L} \text{ and } A_i = \frac{A_i R_o}{R_o + R_L} \qquad \text{.....(42)}$$

Key Point: Here, A_1 is the open loop current gain taking R_L in account.

5. Describe the characteristics Negative feedback. (8)

Transfer Gain:

We have seen, the symbol A is used to represent transfer gain of the basic amplifier without feedback and symbol A_f is used to represent trasnfer gain of the basic amplifier with feedback. Thewse are given as,

$$A = \frac{X_o}{X_i} \text{ and } A_f = \frac{X_o}{X_s}$$

Where X_o = Output voltage or output current

X_i = Input voltage or input current

X_S = Source voltage or source current

As it is negative feedback the relation between X_i and X_S is given as,

$$X_i = X_S + (-X_f)$$

Where X_f = Feedback voltage or feedback current

$$A_f = \frac{X_o}{X_s} = \frac{X_o}{X_i + X_f}$$

Dividing by X_i to numerator and demoniator we get,

$$A_f = \frac{X_o / X_i}{(X_i + X_f)/X_i}$$

$$= \frac{A}{1 + X_f / X_i} \quad \because A = \frac{X_o}{X_i}$$

$$= \frac{A}{1 + (X_f / X_o)(X_o / X_i)}$$

$$\therefore \quad A_f = \frac{A}{1+\beta A} \qquad \because \beta = \frac{X_f}{X_o} \qquad \text{.....(1)}$$

Where β is feedback factor.

Looking at equation we can say that gain without feedback (A) is always greater than gain with feedback (A/(1 + βA) and it decrese with increase in β i.e. increase in feedback factor.

Factor Voltage amplifier, gain with negative feedback is given as,

$$A_{vf} = \frac{A_V}{1 + A_V \beta} \qquad .....(2)$$

Where A_V = Open loop gain i.e. gain without feedback

β = Feedbacl factor

Stability of Gain

The transfer gain of the amplifier is not constant as it depends on the factors such as operating point, temperature etc. This lack of stability in amplifiers can be reduced by introducing negative feedback.

We know that,

$$A_f = \frac{A}{1 + \beta A}$$

Differentiating both sides with respect to A we get,

$$\frac{dA_f}{dA} = \frac{(1+\beta A)1 - \beta A}{(1+\beta A)^2}$$

$$= \frac{1}{(1+\beta A)^2}$$

$$\therefore \qquad dA_f = \frac{dA}{(1+\beta A)^2}$$

Dividing both sides by A_f we get,

$$\frac{dA_f}{A_f} = \frac{dA}{(1+\beta A)^2} \times \frac{1}{A_f}$$

$$= \frac{dA}{(1+\beta A)^2} \times \frac{(1+\beta A)}{A_f} \qquad \text{since } A_f = \frac{A}{1+\beta A}$$

$$\frac{dA_f}{A_f} = \frac{dA}{A} \frac{1}{(1+\beta A)} \qquad .....(3)$$

Where

$\frac{dA_f}{A_f}$ = Fractional Change in amplification with feedback

$\frac{dA}{A}$ = Fractional change in amplification without feedback

Looking at equation (3)we can say that change in the gain with feedback is less than the change in gain without feedback by factor (1+ β A). The fractional change in amplification with feedback divided by fractional change without feedback is called the sensivity of the transfer gain (1 / (1 + β A). The reciprocal of the sensivity is called the desensivity D (1 + β A). The reciprocal of the sensivity is called the desensivity D (1 + β A).

Therefore, stability of the amplifier increases with increase in desensivity.

If $\beta A >> 1$, then

$$A_r = \frac{A}{1+\beta A} = \frac{A}{\beta A}$$

$$= \frac{1}{\beta} \qquad \text{.....}(4)$$

And the gain is dependant only on the feedback network.

Since A reprsents either A_v, G_M, A_1 or R_M and A_f represents the corresponding transfer gains with feedback either A_{vf}, G_M, R_{MF} the equation signifies that:

For voltage series feedback

$$A_{Vf} = \frac{1}{\beta} \text{ Voltage gain is stablized.} \qquad \text{.....}(5)$$

For current series feedback

$$G_{Mf} = \frac{1}{\beta} \text{ Transconduc tan cegain is stablized} \qquad \text{.....}(6)$$

For voltage shunt feedback

$$R_{Mf} = \frac{1}{\beta} \text{ Transeresistor gain is stablized.} \qquad \text{.....}(7)$$

For current shunt feedback

$$A_{if} = \frac{1}{\beta} \text{ current gain is stablized.} \qquad \text{.....}(8)$$

Frequency Response and Bandwidth:

We know that,

$$A_f = \frac{A}{1+\beta A}$$

Using the equation we can write,

$$A_{f\,mid} = \frac{A_{mid}}{1+\beta A_{mid}} \qquad \text{.....}(9)$$

$$A_{f\,low} = \frac{A_{low}}{1+\beta A_{low}} \qquad \text{.....}(10)$$

and $$A_{f\,High} = \frac{A_{high}}{1+\beta A_{high}} \qquad \text{.....}(11)$$

Now we analyze the effect of negative feedback on lower cut-off and upper cut-off frequency of the amplifier.

Lower cut-off frequency:

We know that, the relation between gain at low frequency and gain on mid frequency, is given as,

$$\frac{A_{low}}{A_{mid}} = \frac{1}{1-j\left(\frac{f_t}{f}\right)} \quad \therefore A_{low} = \frac{A_{mid}}{1-j\left(\frac{f_t}{f}\right)}$$

Substituting value of A_{low} in equation (10) we get,

$$A_{f\,low} = \frac{\frac{A_{mid}}{1-j\left(\frac{f_t}{f}\right)}}{1+\beta\left(\frac{A_{mid}}{1-j\left(\frac{f_t}{f}\right)}\right)} = \frac{A_{mid}}{1-j\left(\frac{f_t}{f}\right)+A_{mid}\beta}$$

$$= \frac{A_{mid}}{\left(1+A_{mid}\beta-j\left(\frac{f_t}{f}\right)\right)}$$

Dividing numerator and denominator by $(1 + A_{mids}\,\beta)$ new get,

$$A_{f\,Low} = \frac{\dfrac{A_{mid}}{1+A_{mid}\beta}}{1-j\left(\dfrac{f_t}{\dfrac{1+A_{mid}\beta}{f}}\right)}$$

$$= \frac{A_{f\,mid}}{1-j\left[\left(\dfrac{f_L}{\dfrac{1+A_{mid}\beta}{f}}\right)\right]} \qquad \because A_{f\,mid} = \frac{A_{mid}}{1+A_{mid}\beta}$$

$$\therefore \quad \frac{A_{f\,low}}{A_{f\,mid}} = \frac{1}{1-j\left(\dfrac{f_{Lf}}{f}\right)} \qquad \text{.....(13)}$$

Where

Lower cut-off frequency with feedback

$$= f_{Lf} = \frac{f_L}{1+A_{mid}\beta} \qquad \text{.....(14)}$$

From equation (14), we can say that lower cut-off frequency with feedback is less than lower cut-off frequency without feedback by factor $(1 + A_{mid}\,\beta)$. Therefore, by Introducing negative feedback low frequency response of the amplifier is improved.

Upper cut-off frequency:

We know that, the relation between gain at high frequency and gain at mid frequency is given as,

$$\frac{A_{high}}{A_{mid}} = \frac{1}{1-j\left(\dfrac{f}{f_H}\right)}$$

$$\therefore \quad A_{high} = \frac{A_{mid}}{1-j\left(\dfrac{f}{f_H}\right)} \qquad \text{.....(15)}$$

Substituting value of A_{high} in equation (11) we get,

$$A_{f\,High} = \frac{\dfrac{A_{mid}}{1 - j\left(\dfrac{f}{f_H}\right)}}{1 + \beta\left(\dfrac{A_{mid}}{1 + \left(\dfrac{f}{f_H}\right)}\right)} = \frac{A_{mid}}{1 - j\left(\dfrac{f}{f_H}\right) + A_{mid}\beta}$$

Dividing numerator and denominator by $(1 + A_{mid}\,\beta)$ we get,

$$A_{f\,High} = \frac{\dfrac{A_{mid}}{1 + A_{mid}\beta}}{1 - j\left(\dfrac{f}{(1 + A_{mid}\beta f_H)}\right)}$$

$$A_{f\,High} = \frac{A_{mid}}{1 - j\left[\dfrac{f}{(1 + A_{mid}\beta) f_H}\right]} \qquad \because A_{f\,mid} = \frac{A}{1 + A_{mid}\beta}$$

$$= \frac{A_{mid}}{1 - j\left(\dfrac{f}{f_{Hf}}\right)}$$

Where upper cut-off frequency with feedback is given as,

$$f_{Hf} = (1 + A_{mid}\beta) f_H \qquad \text{.....}(16)$$

From equation (16), we can say that upper cut-off frequency with feedback is greater than upper cut-off frequency without feedback by factor $(1 + A_{mid}\,\beta)$. Therefore, by introducing negative feedback high frequency response of the amplifier is improved.

Bandwidth:

The bandwidth of the amplifier is given as,

BW = Upper cut-off frequency - Lower cut-off frequency

Bandwidth of the amplifier with feedback is given as,

$$BW_f = f_{Hr} - f_{Lf} = (1 + A_{mid}\beta) f_H - \frac{f_L}{(1 + A_{mid}\beta)} \qquad \text{.....}(17)$$

It is very clear that $(f_{Hf} - f_{lf}) > (f_H - f_L)$ and hence bandwidth of amplifier with feedback is greater than bandwidth of amplifier without feedback, as shown in Fig. 3.10.

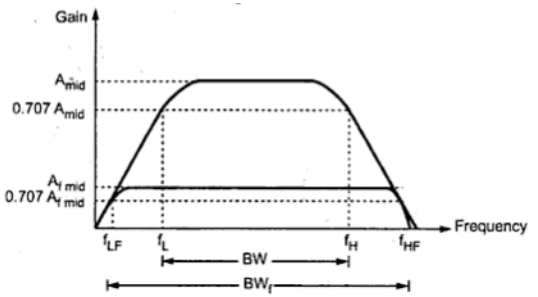


Fig. 3.10 Effect of negative feedback on gain and bandwidth

Frequency Distortion:

Frequency equation (8) we can say that if the feedback network does not contain reactive elements, the overall gain is not a function of frequency. Under such conditions frequency and phase distortion is substantially reduced.

If β is made up of reactive components,reactances of thesse components will change with frequency, changing the β as a result, gain will also change with frequency. This fact is used in turned amplifiers. In turned amplifiers, feedback network is designed such that at turned frequency $\beta \rightarrow 0$ and at other frequencies $\beta \rightarrow \infty$. As a result, amplifier provides high gain for signal at turned frequency and relatively reject all other frequencies.

Noise and Non-linear distortion:

Signal feedback reduces the amount of noise signal and nonlinear distortion. The factor $(1 + \beta A)$ reduces both input and noise and resulting nonlinear distortion also reduced by same factor as the gain.

Input and Output Resistances:

If the feedback signal is added to the input in series with the applied voltage (regardless of whether the feedback is obtained by sampling the output current or voltage), It increases the input resistance. Since the feedback voltage V_f opposes V_S, the input current I_i is less than it would be if V_f were absent, as shown in Fig. 3.11.

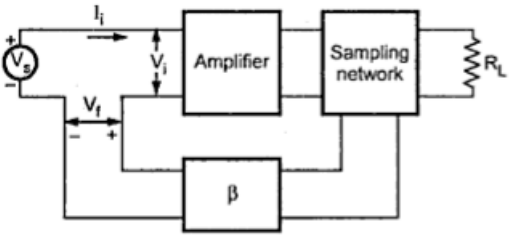


Fig. 3.11

Hence, the input resistance with feedback $R_{if} = \frac{V_s}{I_i}$ is greater than the input resistance without feedback, for the circuit shown in Fig. 3.11.

On the other hand, if the feedback signal is added to the input in shunt with the applied voltage (regardless of whether the feedback is obtained by sampling the output voltage or current). It decreases the input resistance. Since $I_S = I_i + I_f$, the current I_s drawn from the signal source is increased over what if would be if there were no feedback current, as shown in the Fig. 3.12.

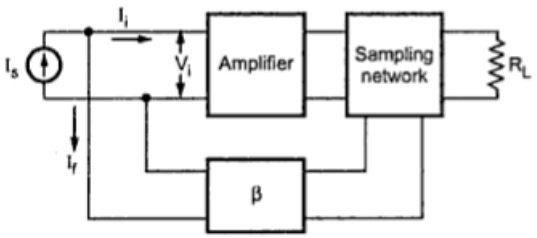


Fig. 3.12

Hence, the input resistance with feedback $R_{if} = \frac{V_i}{I_s}$ is decreased for the circuit shown in Fig.

6. Explain the RC phase shift oscillator with neat diagram
(Nov/Dec 2014, Nov/Dec 2012, Nov/Dec 2011)

For transistor circuit, voltage shunt feedback is employed, the resistance of feedback network will be shunted by low 'R' of the trasnsistor. (Fig. 8.11 (a) and Fig. 8.11 (b)).

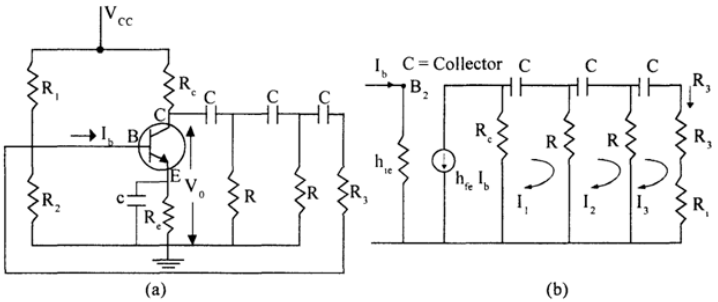


Fig. 8.11 Transistor phase shift oscillator.

The value of $R_3 = R - R_i$ where $R_i \simeq h_{ie}$ the input resistance of transistor. The three RC sections of the phase-shifting network are identical R_1 R_2 and R_e are biasing resistors.

The feedback current $x_f = -I_3$ input current $x_1 = I_b$ (Negative sign is because it is negative feedback)

$$\therefore \text{loop current gain} = \frac{-x_f}{x_i} = \frac{I_3}{I_b}$$

By writing KVL for the three nodes, $\frac{I_3}{I_b}$ can be found out.

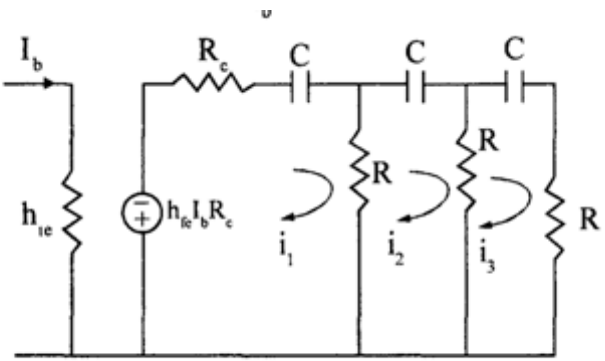


Fig. 8.12 R - C Equivalent circuit.

Loop 1:

$$\left(R_C + R - \frac{j}{\omega c}\right) I_1 - R\, I_2 = -h_{fe}\, I_b\, R_C \qquad \text{.....(1)}$$

Loop 2;

$$-RI_1+\left(2R-\frac{j}{\omega c}\right)I_2-RI_3=0 \qquad .....(2)$$

Loop 3:

$$-RI_2+\left(2R-\frac{j}{\omega c}\right)I_3=0 \qquad .....(3)$$

By taking 'R' as common, the modified given by equations are

$$\left(\frac{R_C}{R}+1-\frac{j}{\omega_{RC}}\right)I_1-I_2=-h_{fe}\,I_b\,\frac{R_C}{R} \qquad .....(4)$$

$$-I_1+\left(2-\frac{j}{\omega RC}\right)I_2-I_3=0 \qquad .....(5)$$

$$-I_2+\left(2-\frac{j}{\omega RC}\right)I_3=0 \qquad .....(6)$$

Let $\frac{R_C}{R}=K$ and $\alpha=\frac{1}{\omega RC}$ the equations are

$$(1+K-j\alpha)I_1-I_2=-h_{fe}\,I_b=0 \qquad .....(7)$$

$$-I_1+(2-j\alpha)I_2-I_3=0 \qquad .....(8)$$

$$-I_2+(2-j\alpha)I_3=0 \qquad .....(9)$$

$$\begin{bmatrix}1+K-j\alpha & -1 & 0\\ -1 & 2-j\alpha & -1\\ 0 & -1 & 2-j\alpha\end{bmatrix}\begin{bmatrix}I_1\\ I_2\\ I_3\end{bmatrix}=\begin{bmatrix}-h_{fe}\,I_b\,K\\ 0\\ 0\end{bmatrix}$$

$$I_3=\frac{1}{\Delta}\begin{vmatrix}1-k-j\alpha & -1 & -h_{fe}I_bK\\ -1 & 2-j\alpha & 0\\ 0 & -1 & 0\end{vmatrix}=\frac{1}{\Delta}\left[-h_{fe}I_bK\right]$$

$$\Delta = \left[1+K-j\alpha\right]\left[\left(2-j\alpha\right)^2-1\right]+\left[-\left(2-j\alpha\right)\right]$$
$$= \left[1+K-j\alpha\right]\left[4-\alpha^2-j4\alpha-1\right]-2+j\alpha$$
$$= -j\alpha^3-j6\alpha-j4K\alpha-5\alpha^2-\alpha^2K+3K+1$$
$$\Delta = -\left(5+K\right)\alpha^2+3K+1+j\left[\alpha^3-\left(6+4K\right)\alpha\right]$$
$$\therefore I_3/I_b = \frac{-h_{fe}\,K}{-\left(5+K\right)\alpha^2+3K+1+j\left[\alpha^3-\left(6+4K\right)\alpha\right]} \qquad .....(10)$$

The Barkhausen condition that the loop gain $\frac{I_3}{I_b}$ phase shift must equal zero. The phase shift equals zero provided imaginary part is zero.

Hence

$$\alpha^3 = \left(6+4K\right)\alpha$$
$$\alpha^2 = 6+4K$$
$$\alpha = \sqrt{6+4K}$$

Since

$$\alpha = \frac{1}{\omega RC}, \qquad \omega = \frac{1}{RC\sqrt{6+4K}}$$

The frequency of oscillations f is given bt

$$f = \frac{1}{2\pi RC\sqrt{6+4K}} \qquad .....(11)$$

For maintaining the oscillations at the above frequency, $\left|I_3/I_b\right| > 1$

$$\left|\frac{I_3}{I_b}\right| = \left|\frac{-h_{fe}\,K}{-\left(5+K\right)\left(6+4K\right)+3K+1}\right| > 1$$
$$\left|-h_{fe}K\right| > \left|-\left(5+K\right)\left(6+4K\right)+3K+1\right|$$
$$\left|-h_{fe}K\right| > \left|-4K^2-23K-29\right|$$
$$h_{fe}K > 4K^2+23K+29$$
$$h_{fe} > 4K+23+\frac{29}{K} \qquad .....(12)$$

To determine the minimum value of h_{fe} , the optimum value of K should be determined by differentiating h_{fe} w.r.t. K and eqyuate it to zero.

$$\frac{dh_{fe}}{dk} > \frac{d}{dk}\left(4K + 23 + \frac{29}{K}\right)$$

$$0 > 4 - \frac{29}{K^2}$$

$$\therefore K^2 < \frac{29}{4}, \qquad \therefore K < 2.7 \qquad \text{.....(13)}$$

Substitute the optimum K = 2.7 in eq. (12)

$$h_{fe} > 4 \times 2.7 + 23 + \frac{29}{2.7}$$

$$\therefore h_{fe} > 44.5 \qquad \text{.....(14)}$$

The BIJ with a small-signal common-emitter short-0circuit gain h_{fe} less than 44.5 cannot be used in this phase shift oscillator.

In R-C phase shift oscillator circuit, each RC network produces 60° phase shift. Thus 3 sections produce the required 180° phase shift. If there are 4-sections, each sections must produce 45° phase shift. But more number of components are to be used. If only 2 sections are these, 90° phase shift must be produced, which is possible for practical B-C network.

7. Explain the operation of a Hartley Oscillator. Derive for its frequency of oscillation. How conditions of oscillations are met? (April/May 2017, Nov/Dec 2016, Nov/Dec 2013, Nov/Dec 2012, Nov/Dec 2011, Nov/Dec 2010)

The amplifier stage uses an active device as a transistor in common emitter configuration. The practical circuit is shown in Fig.4.29.

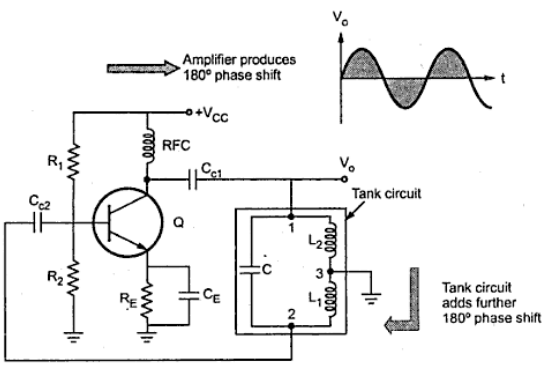


Fig. 4.29 Transistorised Hartley oscillator

The resistance R_1 and R_2 are the biasing resistances. The RFC is the radio frequency choke. Its reactance value is very high frequencies, hence it can be treated as open circuit. While for d.c. conditions, the reactance is zero hence causes no problem for d.c. capacitors.

Hence due to RFC the isolation between a.c. and d.dc operation is achieved. $R_g$is also a biasing circuit resistance and C_g is the emitter bypass operator. C_{C1} and C_{C2} are the coupling operator.

The common emitter provides a phase shift of 180°. As emitter is grounded, the base and the collector voltages are out of phase by 180°. As the centre of L_1 and L_2 is grounded, when upper and becomes positive, the lower becomes negative and viceversa. So the LC feedback network gives an additional phase shift of 180°, necessary to satisfy oscillation conditions.

Derivation of Frequency of Oscillations

The output current which is the collector curent is h_{fe} I_b is the base current. Assuming coupling condensers are short, the capacitor C is between base and collector. The inductance L_1 is between base and emitter while the inductance L_2 is between collector and emitter. Thew equivalent circuit of the feedback network is shown in the fig.4.30

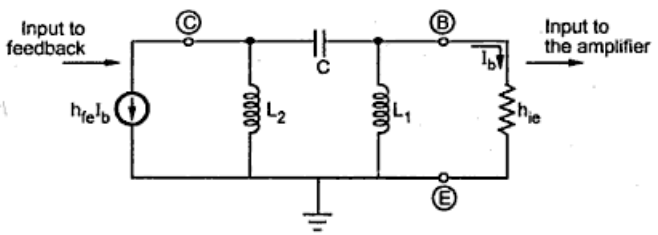


Fig. 4.30 Equivalent circuit

As h_{ie} is the impedance of the transistor. The output of the feedback is the current I_b which is the input current of the trasnsistor. While input to the feedback network is the output of the trasnsitor which is $I_C = h_{fe}$ I_b. converting current into voltage source we get,

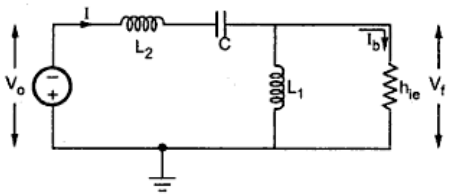


Fig. 4.31 Simplified equivalent circuit

$$V_o = h_{fe} I_b X_{L_2} = h_{fe}\, I_b\, j\omega L_2 \qquad .....(1)$$

Now L_1 and h_{fe} are in parallel, so the total current I drawn from the supply is,

$$I = \frac{-V_o}{\left(X_{L_2} + X_C\right) + \left[X_{L_1} \parallel h_{ie}\right]} \qquad .....(2)$$

Negative sign, as current direction shown in opposite to the polarities of V_o,

Now

$$X_{L_2} + X_C = j\omega L_2 + \frac{1}{j\omega C}$$

Substituting in the equation (2) we get,

$$I = \frac{-h_{fe}\, I_b\, j\omega L_2}{\left[j\omega L_2 + \dfrac{1}{j\omega C}\right] + \dfrac{j\omega L_1\, h_{ie}}{\left(j\omega L_1 + h_{ie}\right)}} \qquad .....(3)$$

Replacing by jω by s,

$$I = \frac{-s\, h_{fe}\, I_b\, L_2}{\left[s L_2 + \dfrac{1}{sC}\right] + \dfrac{s L_1\, h_{ie}}{\left(sL_1 + h_{ie}\right)}}$$

$$= \frac{-s\, h_{fe}\, I_b\, L_2}{\dfrac{\left[1 + s^2 L_2 C\right]}{sC} + \dfrac{sL_1\, h_{ie}}{\left(s L_1 + h_{ie}\right)}}$$

$$= \frac{-s\, h_{fe}\, I_b\, L_2 \left(sC\right)\left(s L_1 + h_{ie}\right)}{\left[1 + s^2 L_2 C\right]\left[s L_1 + h_{ie}\right] + \left(sC\right)\left(s L_1 h_{ie}\right)}$$

$$= \frac{-s^2 h_{fe} I_b L_2 C\left(sL_1 + h_{ie}\right)}{s^3 L_1 L_2 C + sL_1 + h_{ie} + s^2 L_2 C h_{ie} + s^2 L_1 C h_{ie}}$$

$$= \frac{-s^2 h_{fe} I_b L_2 C\left(s L_1 + h_{ie}\right)}{s^3 L_1 L_2 C + s^2 C h_{ie}\left(L_1 + L_2\right) + s L_1 + h_{ie}}$$

According to current division in parallel circuit,

$$I_b = I \times \frac{X_{L_i}}{XL_1 + h_{ie}}$$

$$= I \times \frac{j\omega L_1}{\left(j\omega L_1 + h_{ie}\right)}$$

$$I_b = I \times \left[\frac{s L_1}{\left(sL_1 + h_{ie}\right)}\right] \qquad \text{.....}(4)$$

Substituting value of I from equation (3) in (4),

$$I_b = \frac{-s^2 h_{fe} I_b L_2 C\left(sL_1 + h_{ie}\right)}{\left[s^3\left(L_1 L_2 C\right) + s^2 C h_{ie}\left(L_1 + L_2\right) + sL_1 + h_{ie}\right]} \times \frac{sL_1}{\left(sL_1 + h_{ie}\right)}$$

$$= \frac{-s^3 h_{fe} I_b C L_1 L_2}{s^3\left(L_1 L_2 C\right) + s^2 C h_{ie}\left(L_1 + L_2\right) + sL_1 h_{ie}}$$

$$\therefore \quad 1 = \frac{-S^3 h_{fe} C L_1 L_2}{s^2\left(L_1 L_2 C\right) + s^2 C h_{ie}\left(L_1 + L_2\right) + sL_1 + h_{ie}} \qquad \text{.....}(5)$$

Substituting $s = j\omega$, $s^2 = -\omega^2$, $s^3 = -j\omega^3$ we get

$$\therefore \quad 1 = \frac{j\omega^3 h_{fe} C L_1 L_2}{-j\omega^3 L_1 L_2 C - \omega^2 C h_{ie}\left(L_1 + L_2\right) + j\omega L_1 + h_{ie}}$$

$$= \frac{j\omega^3 h_{ie} C L_1 L_2}{\left[h_{ie} - \omega^2 C h_{ie}\left(L_1 + L_2\right)\right] + j\omega L_1\left(1 - \omega^2 L_2 C\right)} \qquad \text{.....}(6)$$

Rationallsing the R.H.S. of the above equation,

$$\therefore \quad 1 = \frac{j\omega^3 h_{fe} C L_1 L_2\left[h_{ie} - \omega^2 C h_{ie}\left(L_1 + L_2\right) - j\omega L_1\left(1 - \omega^2 L_2 C\right)\right]}{\left[h_{ie} - \omega^2 C h_{ie}\left(L_1 + L_2\right)\right]^2 + \omega^2 L_1^2\left(1 - \omega^2 L_1^2 L_2 C\right)^2} \qquad \text{.....}(7)$$

To satisfy this equation, imaginary part of R.H.S must be zero.

$$\therefore \omega^3 h_{fe} L_1 L_2 C\left[h_{fe} - \omega^2 h_{ie} C\left(L_1 + L_2\right)\right] = 0$$

$$\therefore \omega^3 h_{fe} h_{ie} L_1 L_2 C\left[1 - \omega^2 C\left(L_1 + L_2\right)\right] = 0$$

$$\therefore \quad 1 - \omega^2 C\left(L_1 + L_2\right) = 0$$

$$\therefore \quad \omega^2 = \frac{1}{C\left(L_1 + L_2\right)}$$

$$\therefore \quad \boxed{\omega = \frac{1}{\sqrt{C\left(L_1 + L_2\right)}}}$$

$$\therefore \quad \boxed{f = \frac{1}{2\pi\sqrt{C\left(L_1 + L_2\right)}}}$$

This is the frequency of the oscillations. At this frequency, the restriction of the value of h_{ie} can be obtained, by equating the magnitudes of the both sides of the equation (7).

$$\therefore \quad 1 = \frac{\omega^4 h_{fe} L_1^2 L_2 C\left(1 - \omega^2 L_2 C\right)}{0 + \omega^2 L_1^2 \left(1 - \omega^2 L_2 C\right)^2} \text{ at } \omega = \frac{1}{\sqrt{C\left(L_1 + L_2\right)}}$$

$$\therefore \quad 1 = \frac{h_{fe} L_2}{\left(1 - \omega^2 L_2 C\right)} \text{ at } \omega = \frac{1}{\sqrt{C\left(L_1 + L_2\right)}}$$

$$\therefore \quad 1 = \frac{h_{fe} L_2}{\left[1 - \dfrac{L_2 C}{C\left(L_1 + L_2\right)}\right]} = \frac{h_{fe} L_2}{L_1}$$

$$\therefore \quad \boxed{h_{fe} = \frac{L_1}{L_2}} \qquad \text{.....(9)}$$

This is the value of h_{fe} required to satisfy the oscillating conditions.

For a mutual inductance of M,

$$\boxed{h_{fe} = \frac{L_1 + L_2}{L_2 + M}} \qquad \text{.....(10)}$$

Now $L_1 + L_2$ is the equivalent inductance of the two inductances L_1 and L_2 connected is series defined as

$$\boxed{L_{eq} = L_1 + L_2} \qquad \text{.....(11)}$$

Hence the frequency of oscillations is given by,

$$\boxed{f = \frac{1}{2\pi\sqrt{C L_{eq}}}} \qquad \text{.....(12)}$$

Key Point: So if the capacitor C is kept variable, frequency can be varied over a large range as per the requirement.

In practice, L_1 and L_2 may be wound on a ingle core so that there exists a mutual inductance L_{eq} Hence,

$$\boxed{L_{eq} = L_1 + L_2 + 2M}$$

If L_1 and L_2 are assisting each other then sign of 2M is positive while if L_1 and L_2 are in series opposition then sign of 2M is negative.

The expression for the frequency of the oscillations remain same as given by (12).

A practical circuit where the mutual inductance exist between L_1 and L_2 of transistorized Hartley oscillator is shown in the Fig. 4.30

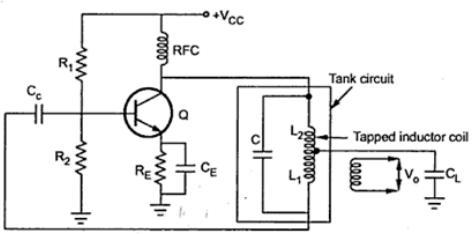


Fig. 4.32 Another form of transistorised Hartley oscillator

Key Point: The Hartley oscillator are widely used in the radio receivers as local oscillators.

8. Explain the operation of a Colpitts Oscillator. Derive for its frequency of oscillation.

An LC oscillator which uses two capacitives reactances and one inductive reactance in the feedback network i.e. tank circuiot, is called colpts oscillator.

The amplifier stage uses an active device as a trasnistor in common enitter configuration. The practical circuit is shown in the Fig. 4.34.

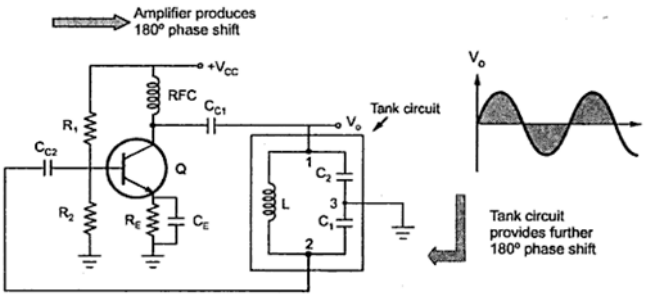


Fig. 4.34 Transistorised Colpitts oscillator

The basic circuit is same as trasnistorised Hartley oscillator, except the tank circuit. The common emitter amplifier causes a sphase shift of 180°, whilke the tank circxuit ads further 180° phase shift, to satisfy the oscillating conditions.

As seen earlier, the output current I_C which is h_{fe} I_b acts as input to the feedback network. While the base current I_b acts as the output current of the tank circuit, flowing through the input impedance of the amplifier h_{ie}. The equivalent circuiot of the tank circuit is shown in the Fig. 4.35.

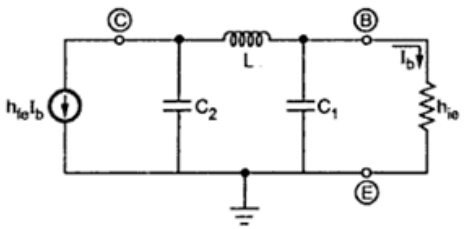


Fig. 4.35 Equivalent circuit

Converting the current source into the voltage source. We get the equivalent circuit as shown in the Fig. 4.36.

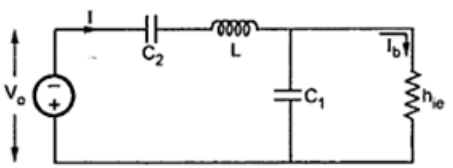


Fig. 4.36 Simplified equivalent circuit

$$V_o = h_{fe} I_b X_{C_2} = h_{fe}\, I_b \frac{1}{j\omega C_2} \qquad \text{.....}(1)$$

The total current I, drawn from the supply is,

$$I = \frac{-V_o}{\left[X_{C_2} + X_L\right] + \left[X_{C_1} \parallel h_{ie}\right]} \qquad \text{.....}(2)$$

The negative sign is because the current direction is assumed in the opposite direction to that, would be due to the polarities of V_o,

Now

$$X_{C2} + X_L = \frac{1}{j\omega C_2} + j\omega L.$$

And

$$X_{C1} \parallel h_{ie} = \frac{\dfrac{1}{j\omega C_1} + h_{ie}}{\left[\dfrac{1}{j\omega C_1} + h_{ie}\right]}$$

Substituting in the equation (4.789),

$$I = \frac{-h_{fe} I_b \left(\dfrac{1}{j\omega C_2}\right)}{\left[\dfrac{1}{j\omega C_2} + j\omega t\right] + \left[\dfrac{\dfrac{h_{ie}}{j\omega C_1}}{h_{ie} + \dfrac{1}{j\omega C_1}}\right]} \qquad \text{.....}(3)$$

Replacing jω by s,

$$I = \frac{-h_{fe} I_b \left(\dfrac{1}{sC_2}\right)}{\left[\dfrac{1}{sC_2} + sL\right] + \left(\dfrac{\dfrac{h_{ie}}{sC_1}}{h_{ie} + \dfrac{1}{sC_1}}\right)}$$

$$= \frac{-h_{ie} I_b \left(\frac{1}{sC_2}\right)}{\frac{\left(1+s^2LC_2\right)}{sC_2} + \left[\frac{h_{ie}}{1+sC_1h_{ie}}\right]}$$

$$= \frac{-h_{fe} I_b \left(\frac{1}{sC_2}\right)(sC_2)(1+sC_1h_{ie})}{(1+s^2LC_2)(1+sC_1h_{ie})+1+sC_2h_{ie}}$$

$$= \frac{-h_{ie} I_b (1+sC_1 h_{ie})}{s^3 LC_1C_2 h_{ie} + s^2 LC_2 + sC_1h_{ie} + 1 + sC_2 h_{ie}}$$

$$= \frac{-h_{fe} I_b (1+sC_1 h_{ie})}{s^3 LC_1C_2 h_{ie} + s^2 LC_2 + s h_{ie}(C_1+C_2) + 1} \quad \text{.....(4)}$$

According to the current division in the parallel circuit,

$$I_b = 1 \times \frac{X_{C_1}}{\left(X_{C_1} + h_{ie}\right)} = \frac{1 \times \frac{1}{j\omega C_1}}{\left(h_{ie} + \frac{1}{j\omega C_1}\right)}$$

$$\therefore \quad I_b = \frac{1}{(1+s h_{ie} C_1)}$$

Substituting value of 1 from the equation (4), in (5), we get

$$= \frac{-h_{ie} I_b (1+sC_1 h_{ie})}{s^3 LC_1C_2 h_{ie} + s^2 LC_2 + s h_{ie}(C_1+C_2) + 1} \times \frac{1}{(1+sC_1 h_{ie})}$$

$$= \frac{-h_{fe} I_b}{s^3 LC_1C_2 h_{ie} + s^2 LC_2 + s h_{ie}(C_1+C_2) + 1}$$

$$1 = \frac{-h_{ie}}{s^3 LC_1C_2 h_{ie} + s^2 LC_2 + s h_{ie}(C_1+C_2) + 1} \quad \text{.....(6)}$$

Replacing s by jω, and S^2 by $-\omega^2$ and S^3 by $-j\omega^3$

$$1 = \frac{-h_{fe}}{-j\omega^3 LC_1C_2h_{ie} - \omega^2 LC_2 + j\omega h_{ie}(C_1+C_2) + 1}$$

$$= \frac{-h_{fe}}{(1-\omega^2 LC_2) + j\omega h_{ie}\left[C_1 + C_2 - \omega^2 LC_1C_2\right]} \quad \text{.....(7)}$$

There is no need to rationalize this as there are no j terms in the numerator, as in the equation (6 of 4.10.2)

It can be seen that, to satisfy the equation, the imaginary part of the denominator of tehj right hand side must be zero.

$$\therefore \quad \omega h_{ie}\left[C_1 + C_2 - \omega^2 L C_1 C_2\right] = 0$$

$$\therefore \quad C_1 + C_2 - \omega^2 L C_1 C_2 = 0$$

$$\therefore \quad \omega^2 = \frac{(C_1 + C_2)}{L C_1 C_2} = \frac{1}{L\left[\frac{C_1 C_2}{(C_1 + C_2)}\right]}$$

$$\therefore \quad \boxed{\omega = \frac{1}{\sqrt{L\left[\frac{C_1 C_2}{(C_1 + C_2)}\right]}}}$$

Now $\frac{C_1 C_2}{C_1 + C_2}$ is nothing but the equivalent of two capacitors C_1 and C_2 in series.

$$\therefore \quad \boxed{C_{eq} = \frac{C_1 C_2}{C_1 + C_2}}$$

$$\therefore \quad \boxed{\omega = \frac{1}{\sqrt{L C_{eq}}}} \qquad .....(8)$$

$$\therefore \quad \boxed{f = \frac{1}{2\pi\sqrt{L C_{eq}}}} \qquad .....(9)$$

This is the frequency of the oscillations in the Colpitts oscillator.

Substituting this frequency in the equation (7) and equating the magnitudes of the both sides, the restriction on the value of h_{fe} can be obtained as,

$$\boxed{h_{ie} = \frac{C_2}{C_1}} \qquad .....(10)$$

Thus the behavior of Colpitts oscillator is similar to the Hartley oscillator, as basic LC oscillator circuit is same, except the tank circuit.

Key Point: The Colpitts oscillator is very commonly used as local oscillator in superheterodyne radio receiver.

9. Explain the operation of a Crystal Oscillator. Derive for its frequency of oscillation.

The crystals are either naturally occurring or synthetically manufactured, exhibiting the piezoelectric effect. The piezoelectric effect means under the influence of the mechanical pressure, the voltage gets generated across the opposite faces of the crystal.

If the mechanical force is applied in such a way to force the crystal to vibrate, the a.c. voltage gets generated across it. Conversely, if the crystal is subjected to a.c. voltage, it vibrates causing mechanical distortion in the crystal shape.

Every crystal has its own resonating frequency depending on its cut. So under the influence of the mechanical vibrations, the crystal generates an electrical signal of very constant frequency. The crystal has a greater stability in holding the constant frequency. A crystal oscillator is basically a tuned-circuit oscillator using a piezoelectric crystal as its resonant tank circuit. The crystal oscillators are preferred when greater frequency stability is required. Hence the crystals are used in watches, communication transmitters and receivers etc. The main substances exhibiting the piezoelectric effect are quartz, Rochelle salt and tourmaline.

Rochelle salts have the greatest piezoelectric activity. For a given a c. voltage, they vibrate more than quartz or tourmaline. Hence these are preferred in making microphones associated with portable tape recorders, headsets, loudspeakers etc. Rochelle salt is mechanically weakest of the three and break very easily. Tourmaline shows least piezoelectric effect but mechanically strongest. The tourmaline is most expensive and hence its use is rare in practice

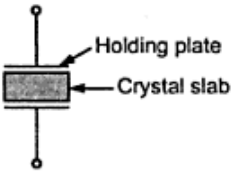
Quartz is a compromise between the piezoelectric activity of Rochelle salts and the strength of the tourmaline. Quartz is inexpensive and easily available in nature and hence very commonly used in the crystal oscillators.

Key Points: Quartz is widely used for RF oscillators and the flters.

Construction Details:

The natural shape of a quartz crystal is a hexagonal prism. But for its practical use, It si cut to the rectangular slab. This slab is then mounted between the two mutual plates. The symbolic representation of such a practical crystal is shown in the Fig. below. The metal plates are called holding plates, as they the crystal slab in between them.

Constructional Details



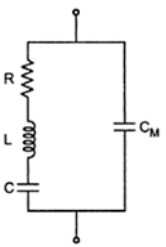
Symbolic representation of a crystal

A.C Equivalent Circuit

When the crystal is not vibrating, it is equivalent to a capacitance due to the mechanical mounting of the crystal such a capacitance existing due to the two metal plates separated by a dielectric like crystal slab, is called mounting capacitance denoted as C_M or C.

When it is vibrating, there are internal frictional losses which are denoted by a resistance R. While the mass of the crystal, which is indication of its inertia is represented by an inductance L. In vibrating condition, it is having some stiffness, which is represented by a capacitor C.

The mounting capacitance is a shunt capacitance. And hence the overall equivalent circuit of a crystal can be shown in the Fig. below



A.C equivalent circuit of a crystal

RLC forms a resonating circuit. The expression for the resonating frequency f_r is ,

$$f_r = \frac{1}{2\pi\sqrt{LC}}\sqrt{\frac{Q^2}{1+Q^2}} \qquad \text{.....(1)}$$

Where Q = quality factor of crystal

$$\therefore \quad Q = \frac{\omega L}{R} \qquad \text{.....(2)}$$

The Q factor of the crystal is very high, typically 20,000 value of Q upto 10^6 also can be achieved. Hence $\sqrt{\frac{Q^2}{1+Q^2}}$ factor approaches to unit and we get the resonating frequency as,

$$\boxed{f_r = \frac{1}{2\pi\sqrt{LC}}} \qquad \text{.....}(3)$$

The crystal frequency is infact inversely proportional to the thickness of the crystal.

$$\boxed{f = \frac{1}{\tau}} \quad \text{where t = thickness}$$

So to have very high frequencies, thickness of the crystal should be very small . But it makes the crystal mechanically weak an hence it may get damaged, under the vibrations. Hence practically crystal oscillators are used 200 or 300 kHz only.

The crystal has two resonating frequencies, series resonant frequency and paralled resonant frequency.

Series and parallel Resonance:

Once resonant condition occurs when the reactances of series RLC leg are equal i.e. $X_L = X_C$. This is nothing but the series resonance. The impedance offered by this branch, under resonant condition is minimum which is resistance R. The series resonance frequency is same as the resonating frequency given by the equation (3).

$$\boxed{f_s = \frac{1}{2\pi\sqrt{LC}}}$$

The other resonant condition occurs when the reactances of series resonant leg equals the reactanceof the mounting capacitor C_M. This is parallel resonance or antiresonance condition.

Under this condition the impedance offered by the crystal to the external circuit is maximum.

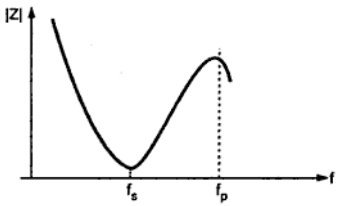
Under parallel resonance, the equivalent capacitance is,

$$C_{eq} = \frac{C_M C}{C_M + C} \qquad .....(5)$$

Hence the parallel resonating frequency is given by,

$$\boxed{f_p = \frac{1}{2\pi\sqrt{L C_{eq}}}} \qquad .....(6)$$

When the crystal capacitance C is much smaller than C_M, then the Fig. shows the behavior of crystal impedance versus frequency.



Crystal impedance versus frequency

Generally values of f_s and f_p are very close to each other and practically it can be said that there exists only one resonating frequency for a crystal.

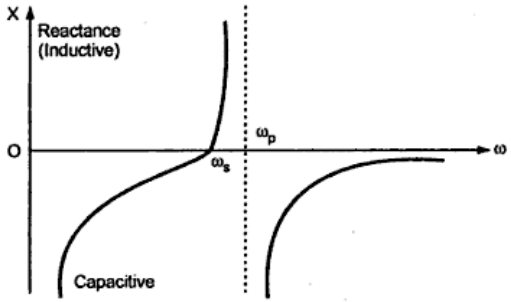
The higher value of Q is the m,ain advantage of crystal. Due to high Q of a resonant circuit, it provides very good frequency stability. If we neglect the resistance R, the impedance of the crystal is a reactance jX which depends on the frequency as,

$$jx = \frac{j}{\omega C_M} \cdot \frac{\omega^2 - \omega_s^2}{\omega^2 - \omega_P^2}$$

Where ω_s = series resonant frequency

ω_p = Parallel resonant frequency

The sketch of reactance against frequency is shown in the Fig. below



The reactance versus frequency

The oscillating frequency lies between ω_s sand ω_p.

Crystal Stability:

The frequency of the tends to change slightly with time due to temperature, against etc.

i) Temoperature Stability: It is defined as the change in the frequency per degree change in the temperature. This is Hz/MHz/°C. For 1°C change in the temperature, the frequency changes by 10 to 12 Hz in MHz. This is neglibly small. So for all practical purpose it is treated to be constant. But if this much change is also not acceptable then the crystal is kept in box where temperature is maintained constant, called constant temperature box.

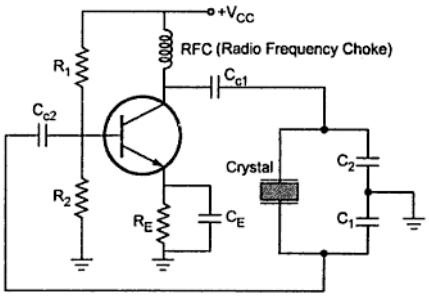
ii) Long term stability: It is basically due to aging of the crystal material. Aging rates are 2×10^{-8} per year, for a quartz crystal, the frequency drift with time is, typically less than 1in 10^6 i.e. 0.0001° % per day. This is also very small.

Key Point: Overall crysrtal has good frequency stability. Hence it is used in computers, counrters, basic timing devices in electronic wrist watches, etc.

Pierce Crystal Oscillator:

The Colpitts oscillator can be modified by using the crystal to behave as an inductior. The circuit is called pierce crystal oscillator. The crystal behaves as an inductor for a frequency slightly higher than the series resonance frequency f_s. Th two capacitors C_1, C_2 requierd in trhe tank circuit along with an inductor are used, as they are used in Coipitts oscillator circuit. As

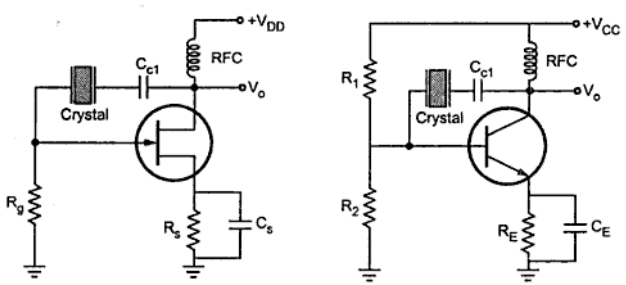
only inductor gets replaced by the crystal, which behaves as an inductor, the basic working principle of pierce crystal oscillator is same as that of Colpitts oscillator. The practical transistorised pierce crystal oscillator circuit is shown in the Fig. below



The resistances R1, R2, R_E provide d c. bias while the capacitor C_E is emitter bypass capacitor. RFC (Radio Frequency Choke) provides isolation between a c. and d.c operation.C_{c1} and C_{c2} are coupling capacitors.

The resulting circuit frequency is set by the series resonant frequency of the crystal, Change in the supply voltages, temperature, transistor parameters have no effect on the circuit operating conditions and hence good frequency stability is obtained.

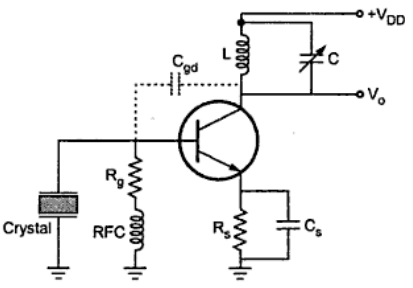
The oscillator circuit can be modified by using the internal capacitors of the transistor used instead of C_1 and C_2. The separate capacitors C_1, C_2 are not required in such circuit. Such circuits using FET and transistor are shown in the Fig. (a) and (b).



Pierce crystal oscillator

Miller Crystal oscillator

Similar to the modifications in Colpitts oscillator, the Hartley oscillator circuit can be modified, to get Miller crystal oscillator. In Hartley oscillator circuit, two inductors and one capacitor is required in the tank circuit. One inductor is replaced by the crystal which acts as an inductor for the frequencies slightly greater than Crystal the series resonant frequency. The transistorized Miller crystal oscillator circuit is shown in the Fig.



Miller crystal oscillator

The tuned circuit of L_1 and C is off tuned to behave as an inductor ie. Ln. The crystal behaves as other inductance L_2 between base and ground. The internal capacitance of the transistor acts as a capacitor required to fulfill the elements of the rank circuit. The crystal decides the operating frequency of the oscillator.

10. Explain the operation of a Wien Bridge Oscillator. Derive for its frequency of oscillation. (April/May 2017)

Wien Bridge oscillator

Generally in an oscillator, amplifier stage introduces 180° phase shift and feedback network introduces additional 180° phase shift, to obtain a phase shift of 360° (2π radians) around a loop. This is required condition for any oscillator. But Wien bridge oscillator uses a noninverting amplifier and hence does not provide any phase shift during amplifier stage. As total phase shift required is 0°or 2nx radians, in Wien bridge type no phase shift is necessary through feedback.

Key Point : Thus the total phase shift around a loop is 0°.

Let us study the basic version of the Wien bridge oscillator and its analysis. A basic Wien bridge used in this oscillator and an amplifier stage is shown in the Fig. 4.13

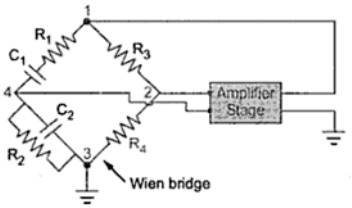


Fig. 4.13 Basic circuit of Wien bridge oscillator

The output of the amplifier is applied between the terminals 1 and 3, which is the input to the feedback network. While the amplifier input is supplied from the diagonal terminals 2 and 4. which is the output from the feedback network. Thus amplifier supplied its own input through the Wien bridge as a feedback network. The two arms of the bridge, namely R1, C1 in series and R2, C2 in parallel are called frequency sensitive arms. This is because the components of these two arms decide the frequency of the Oscillator.

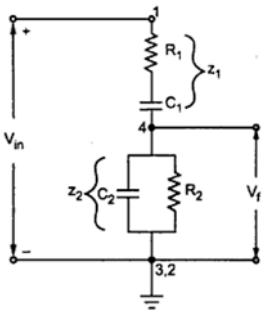


Fig. 4.14 Feedback network of Wien bridge oscillator

Let us find out the gain of the feedback network. As seen earlier input V_{in} to the feedback network is between 1 and 3 while output Vf of the feedback network is between 2 and 4. This is shown in the Fig. 4.14.Such a feedback network is called lead-lag network. This is because at very low frequencies it acts like lag network. Now from the fig.4.14 as shown,

$$\boxed{Z_1 = R_1 + \frac{1}{j\omega C_1} = \frac{1 + j\omega R_1 C_1}{j\omega C_1}}$$

$$Z_2 = R_2 \,||\, \frac{1}{j\omega C_2} = \frac{R_2 \times \dfrac{1}{j\omega C_2}}{R_2 + \dfrac{1}{j\omega R_2 C_2}}$$

$$\therefore \quad \boxed{Z_2 = \frac{R_2}{1 + j\omega R_2 C_2}} \qquad \text{.....(1)}$$

Replacing $j\omega = s$,

$$\boxed{Z_1 = \frac{1 + s R_1 C_1}{s C_1}}$$

and $$\boxed{Z_2 = \frac{R_2}{1 + s R_2 C_2}}$$

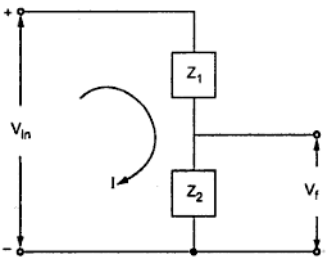


Fig. 4.15 Simplified circuit

$$I = \frac{V_m}{Z_1 + Z_2}$$

$$V_f = I Z_2$$

$$\therefore \quad V_f = \frac{V_m Z_2}{Z_1 + Z_2}$$

$$\therefore \quad \boxed{\beta = \frac{V_r}{V_m} = \frac{Z_2}{Z_1 + Z_2}} \qquad \text{.....(2)}$$

Substituting the value of Z_1 and Z_2,

$$\beta = \frac{\left[\dfrac{R_2}{1 + sR_2 C_2}\right]}{\left[\dfrac{1 + sR_1 C_1}{sC_1}\right] + \left[\dfrac{R_2}{1 + sR_2 C_2}\right]}$$

$$\beta = \frac{sC_1 R_2}{(1 + sR_1 C_1)(1 + sR_2 C_2) + sC_1 R_2}$$

$$= \frac{sC_1R_2}{1+s\left(R_1C_1+R_2C_2\right)+s^2R_1R_2C_1C_2+sC_1R_2}$$

$$= \frac{sC_1R_1}{1+s\left(R_1C_1+R_2C_2+C_1R_2\right)+s^2R_1R_2C_1C_2}$$

Replacing s by jω, $s^2 = -\omega^2$

$$\beta = \frac{j\omega C_1R_2}{\left(1-\omega^2R_1R_2C_1C_2\right)+jGw\left(R_1C_1+R_2C_2+C_1R_2\right)} \quad .....(3)$$

Rationalising the expression,

$$\beta = \frac{j\omega C_1R_2\left[\left(1-\omega^2R_1R_2C_1C_2\right)-j\omega\left(R_1C_1+R_2C_2+C_1R_2\right)\right]}{\left(1-\omega^2R_1R_2C_1C_2\right)^2+\omega^2\left(R_1C_1+R_2C_2+C_1R_2\right)^2}$$

$$\boxed{\beta = \frac{\omega^2C_1R_2\left(R_1C_1+R_2C_2+C_1R_2\right)+j\omega C_1R_2\left(1-\omega^2R_1R_2C_1C_2\right)}{\left(1-\omega^2R_1R_2C_1C_2\right)^2+\omega^2\left(R_1C_1+R_2C_2+C_1R_2\right)^2}} \quad .....(4)$$

To have zero phase shift of the feedback network, is imaginary part must be zero.

$$\therefore \quad \omega\left(1-\omega^2R_1R_2C_1C_2\right)=0$$

$$\therefore \quad \omega^2 = \frac{1}{R_1R_2C_1C_2} \text{ neglecting zero value.}$$

$$\boxed{\omega = \frac{1}{\sqrt{R_1R_2C_1C_2}}}$$

$$\therefore \quad \boxed{f = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}}$$

Key Points: This is the frequency of the oscillator and it shows that the components of the frequency sensitive arms are the deciding factors, for the frequency.

In practice $R_1 = R_2 = R$ and $C_1 = C_2 = C$ are selected.

$$\therefore \quad f = \frac{1}{2\pi\sqrt{R^2C^2}}$$

$$\boxed{f = \frac{1}{2xRC}} \quad .....(6)$$

At $R_1 = R_2 = R$ and $C_1 = C_2 = C$ the feedback network becomes,

$$\beta = \frac{\omega^2 R\,C(3RC) + j\omega RC\left(1-\omega^2R^2C^2\right)}{\left(1-\omega^2R^2C^2\right)+\omega^2(3RC)^2}$$

Substituting $f = \frac{1}{2xRC}$ i.e $\omega = \frac{1}{RC}$

We get the magnitude of the feedback network at the resonating frequency of the oscillator as,

$$\beta = \frac{3}{0+\frac{1}{R^2C^2}\times(3RC)} = \frac{3}{9}$$

$$\therefore \quad \boxed{\beta = \frac{1}{3}} \qquad .....(7)$$

The positive sign of β indicates that the phase shift by the feedback network is 0°. Now to satisfy the Barkhausen criterion for the sustained oscillators, we can write,

$$|A\beta| \geq 1$$

$$\therefore \quad |A| \geq \frac{1}{|\beta|} \geq \frac{1}{\left(\frac{1}{3}\right)}$$

$$\therefore \quad \boxed{|A| \geq 3}$$

This is the required gain of the amplifier stage, without any phase shift.

If $R_1 = R_2$ and $C_1 \neq C_2$ then

$$\boxed{f = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}}$$

Substituting in the equation (4) we get,

$$\boxed{\beta = \frac{C_1R_2}{(R_1C_1 + R_2C_2 + C_1R_2)}}$$

$$|A\beta| \geq 1$$

$$\therefore \quad \boxed{A \geq \frac{R_1C_1 + R_2C_2 + C_1R_2}{C_1R_2}} \qquad .....(8)$$

Another important advantage of the Wien bridge oscillator is that by varying the two capacitor values simultaneously, by mounting them on the common shift, different frequency ranges can be provided.

Let us see the various versions of the Wien bridge oscillator by considering various circuits for the amplifier stage.

Transistorized Wien Bridge Oscillator:

In this circuit, two stage common emitter transistor amplifier is used. Each stage contributes 180° phase shift hence the total phase due to the amplifier stage becomes 360° i.e. 0° which is necessary as per the oscillator conditions.

The practical, transistorized Wien bridge oscillator circuit is shown in the Fig. 4.16.

The bridge consists of R and C in parallel, R_3 and R_4. The feedback is applied from the collector of Q_2 through the coupling capacitor, to the bridge circuit.

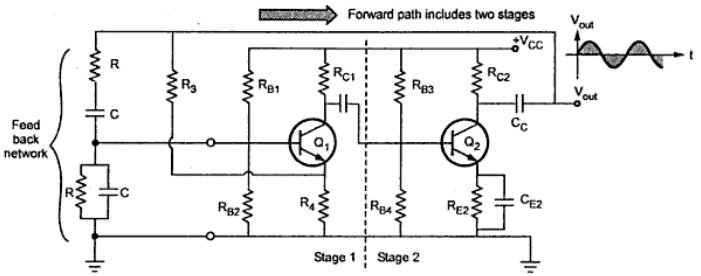


Fig. 4.16 Transistorised Wien bridge oscillator

The resistance R_4 serves the dual purpose of emitter resistance of the transistor Q_1 and also the element of the Wienm bridge.

The two stage amplifier provides a gain much than 3 and it is necessary to reduce it. To reduce the gain, the feedback is used without bypassing the resistance R_4. The negative feedback can accomplish the gain stability and can control the output magnitude. The negative feedback also reduces the distortion and therefore output obtained is a pure sinusoidal in nature. The amplitude stability can be improved using a nonlinear resistor for R_4. Due to this, the loop gain depends on the amplitude of the oscillations. Increase in the amplitude of the oscillations, Increase the current through nonlinear resistance. Which results into an increase inb the value of

nonlinear resistance R_4. When this value increases, a greater amount of negative feedback is applied. This reduces the loop gain. And hence signal amplitude gets reduced and controlled.

11. Compare RC Phase Shift Oscillator with Wien Bridge Oscillator

Sl. No.	RC Phase shift Oscillator	Wien Bridge Oscillator
1)	It is a phase shift oscillators used for low frequency range.	It is also a phase shift oscillator used for low frequency range.
2)	The feedback network is RC network with three RC sections.	The feedback network is lead-lag network which is called Wien bridge circuit.
3)	The feedback network introduces 180° phase shift.	The feedback network does not introduce any phase shift.
4)	Op-amp is used in an inverting mode.	Op-amp is used in non-inverting mode.
5)	Op-amp circuit introduces 180° phase shift.	Op-amp circuit does not introduces any phase shift.
6)	The frequency of oscillations is , $f = \frac{1}{2\pi RC\sqrt{6}}$	The frequency of oscillations is , $f = \frac{1}{2\pi RC}$
7)	The amplifier gain condition is, $\lvert A \rvert \geq 29$	The amplifier gain condition is, $\lvert A \rvert \geq 3$
8)	The frequency variation is difficult.	Mounting the two capacitors on common shaft and varying their values, frequency can be varied.